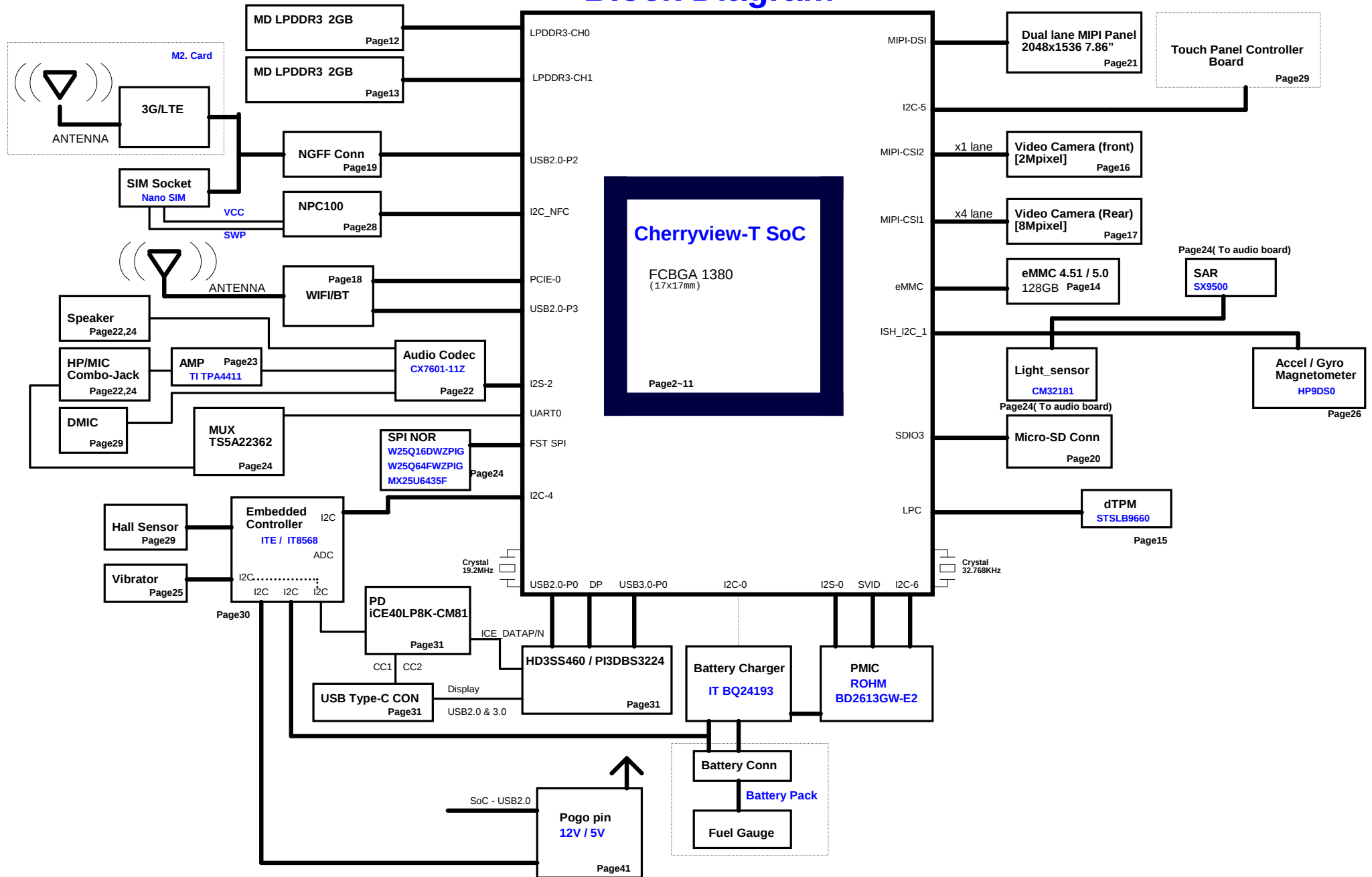
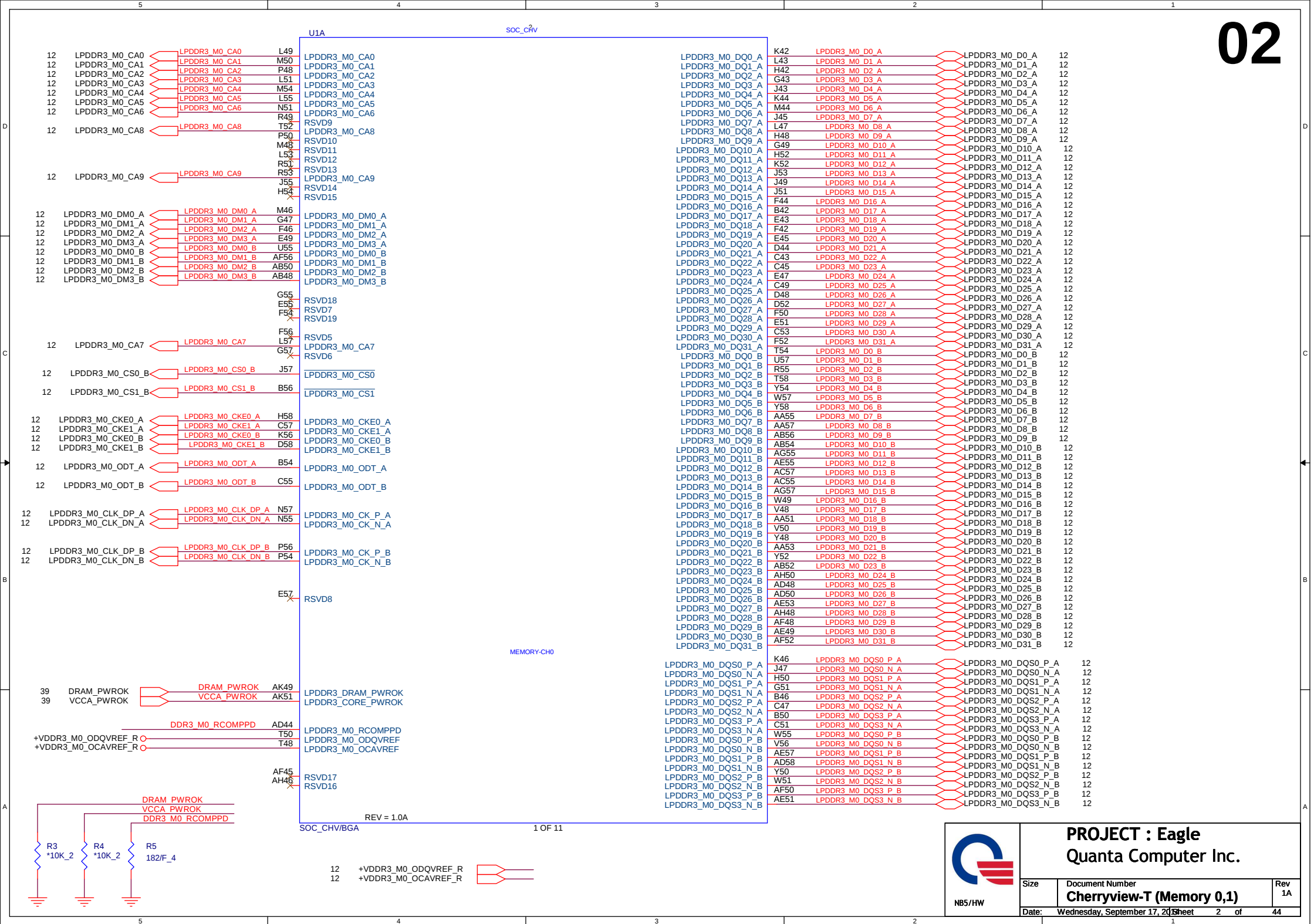
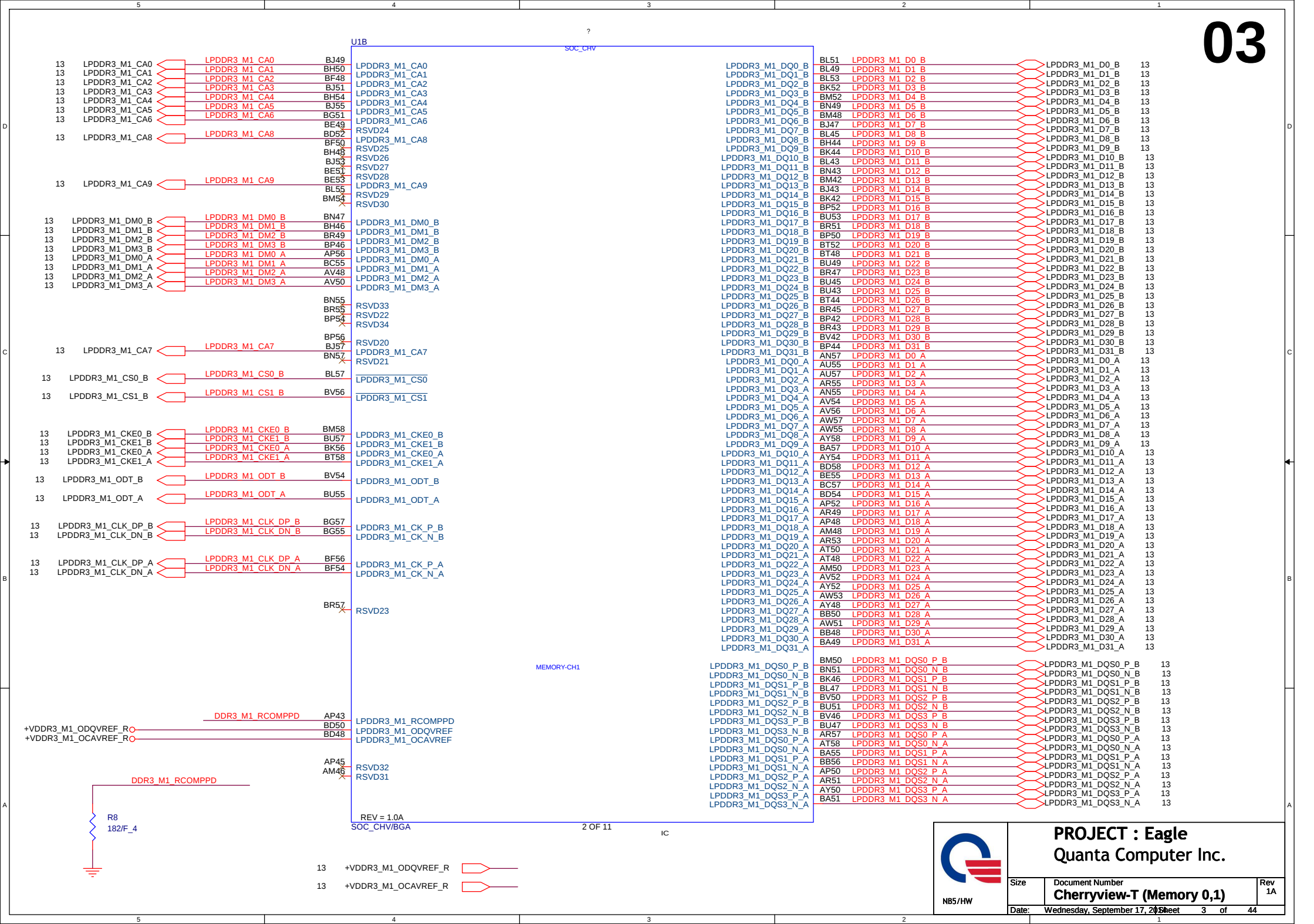


Intel Cherry Trail-T Platform Block Diagram

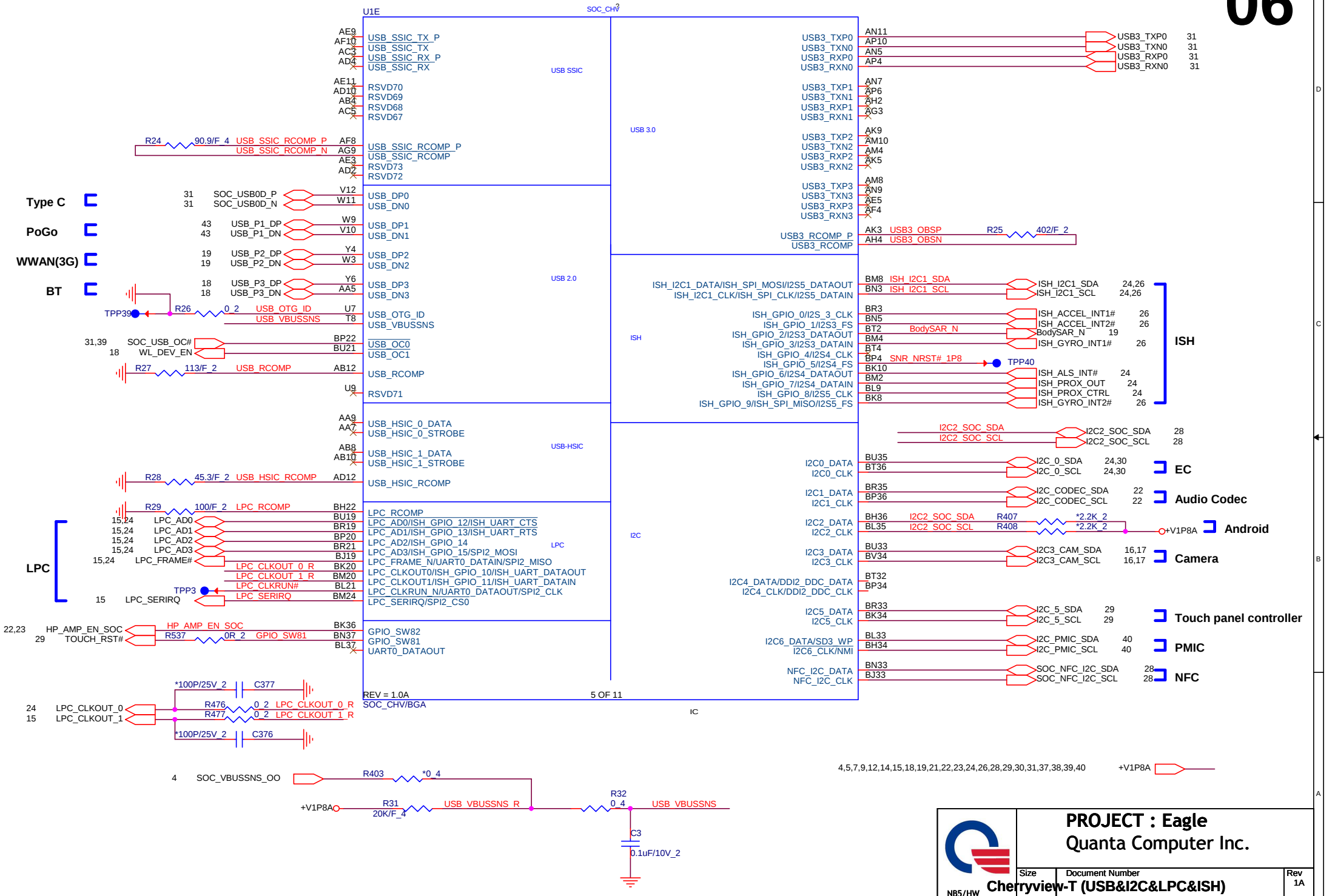


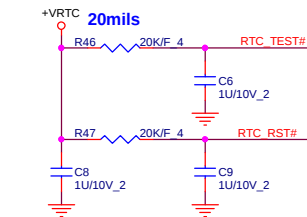
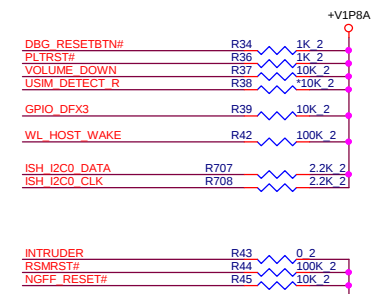
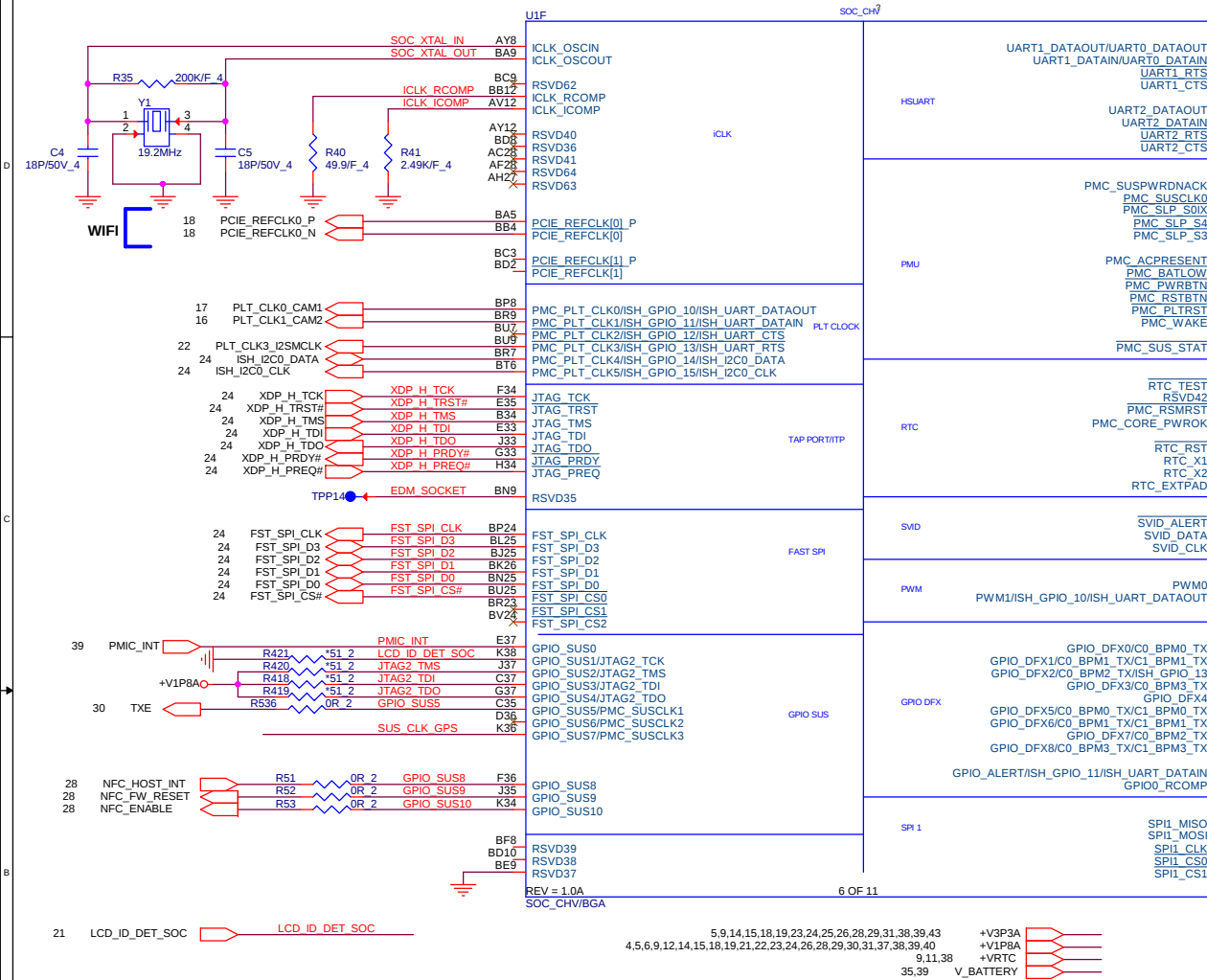




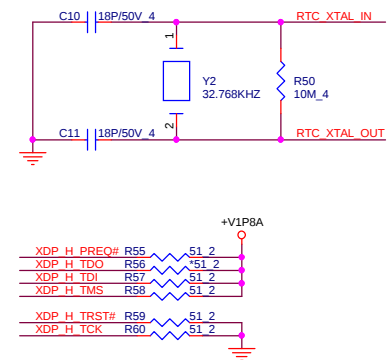






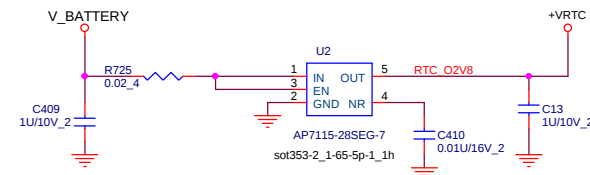


RTC Clock 32.768KHz



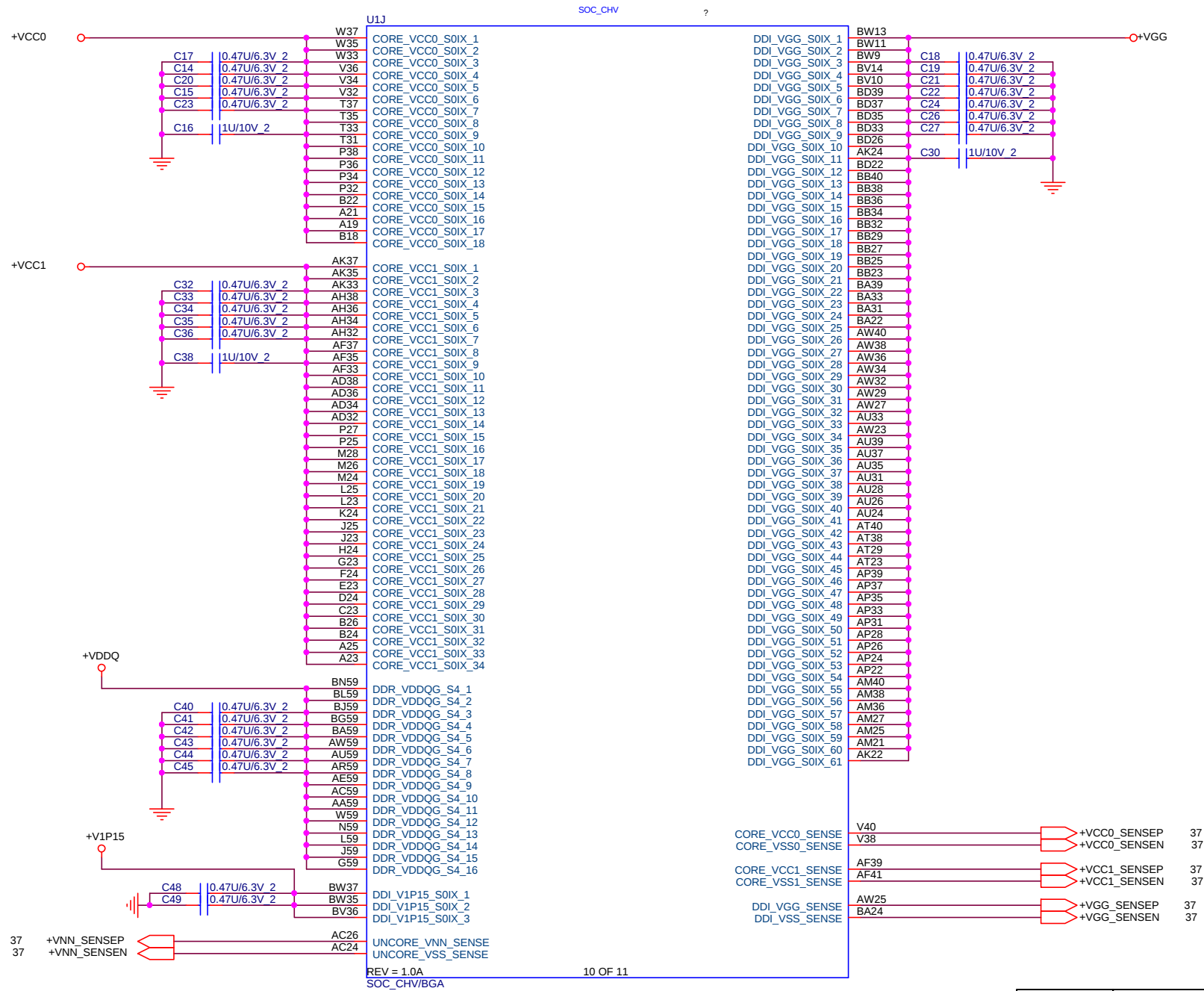
Hardware Strap (EDS1P0)

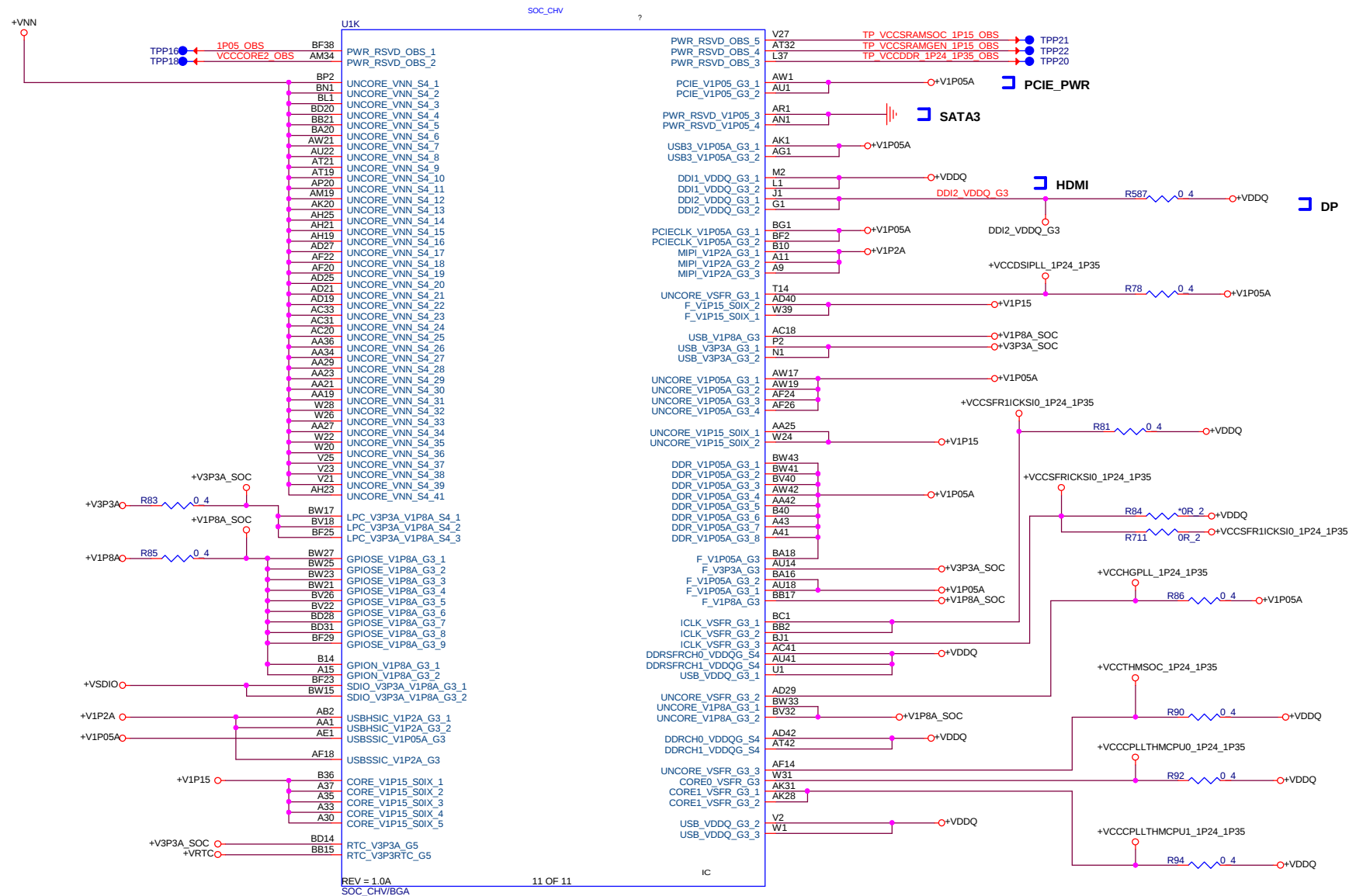
Pin Name	Purpose	Polarity	Internal PU/PD	
GPIO_SUS0	DDI0 Detected	0 = Port DDI0 is not detected 1 = Port DDI0 is detected	PD	+V1P8A R61 *10K 2 PMIC_INT
GPIO_SUS5	Flash Descriptor Security Override	0 = Override 1 = Normal Operation	PU	R64 *2K 4 GPIO_SUS5
GPIO_SUS7	DFX Sus Debug Strap	0 = SUS Debug 1 = No SUS Debug	PU	+V1P8A R66 *10K 2 SUS_CLK_GPS R67 2K 4
GPIO_SUS8	SFR Supply Select	0 = Supply is 1.25V 1 = Supply is 1.35V	PD	+V1P8A R68 *10K 2 GPIO_SUS8 R69 2K 4
GPIO_SUS9	ICLK, USB2, DDI SFR Bypass	0 = Use LDOs 1 = Bypass LDOs (supply 1.05V on power pins)	PD	+V1P8A R71 *10K 2 GPIO_SUS9
GPIO_SUS10	POSM Select	0 = Fuse Controller 1 = PMC	PD	+V1P8A R73 *10K 2 GPIO_SUS10



PROJECT : Eagle
Quanta Computer Inc.

Size	Document Number	Rev
	Cherryview-T (CLK/UART/SPI/PMU)	1A
Date:	Wednesday, September 17, 2014	Sheet 7 of 44



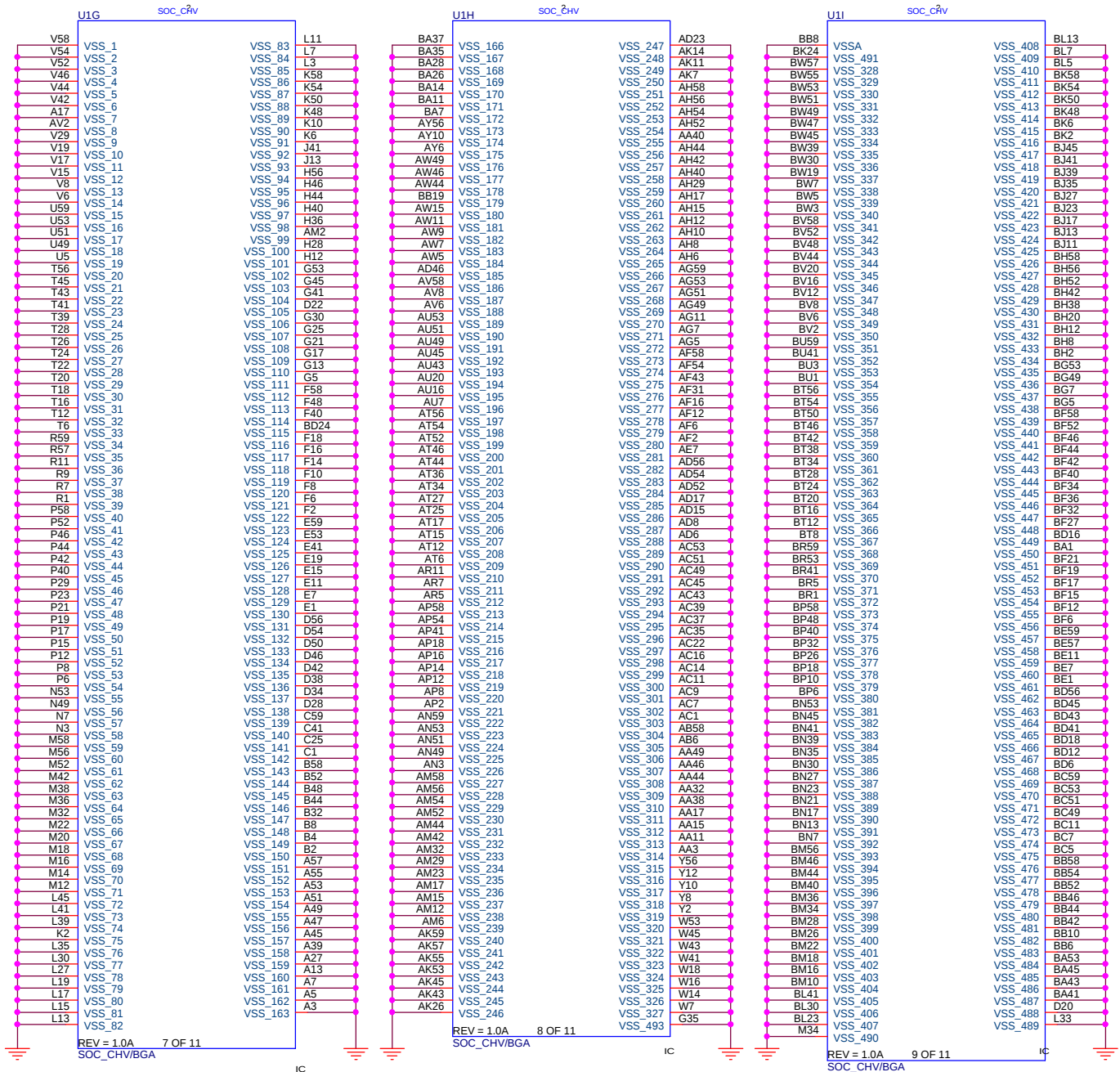


11,37	+VNN
5,14,15,18,19,23,24,25,26,28,29,31,38,39,43	+V3P3A
11,38	+V1P8A
11,38	+VSDIO
11,38	+V1P2A
11,37,38	+V1P05A
8,11,24,37	+V1P15
7,11,38	+VRTC
8,11,12,13,37,38	+VDDQ



PROJECT : Eagle
Quanta Computer Inc.

Size	Document Number	Rev
	Cherryview-T (POWER 2/2)	1A
Date:	Wednesday, September 17, 2014	9 of 44



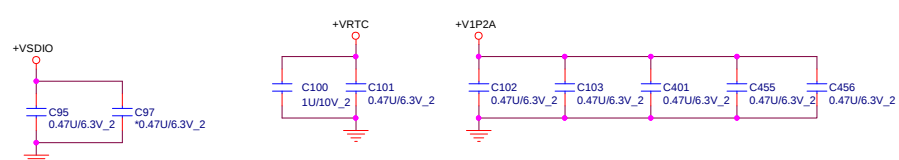
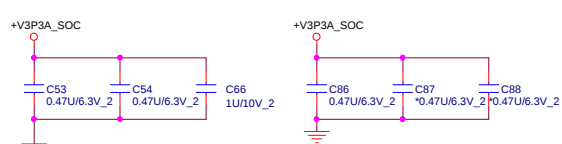
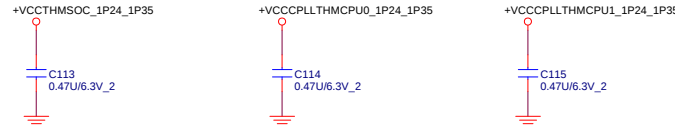
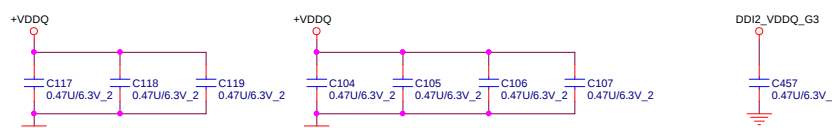
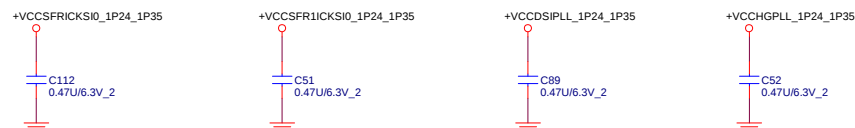
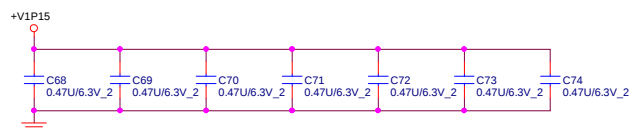
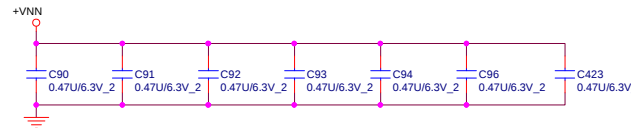
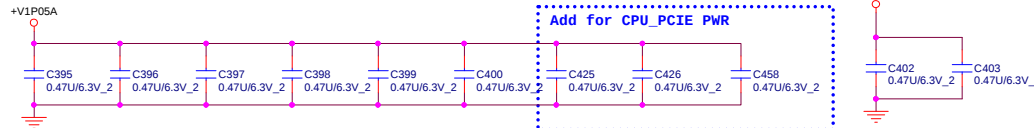
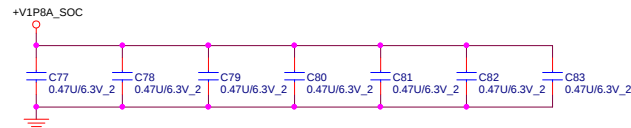
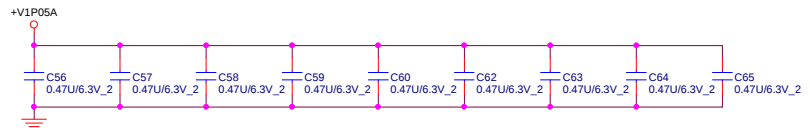
QBCON	TOPB/S	Vender PN
AJ0QH7BUT01	AJ0QH7BUT00	2.0G QH7B
AJ0QH7CUT01	AJ0QH7CUT00	2.0G QH7C
AJ0QHAUUT01	AJ0QHAUUT00	2.16G QHAU



NB5/HW

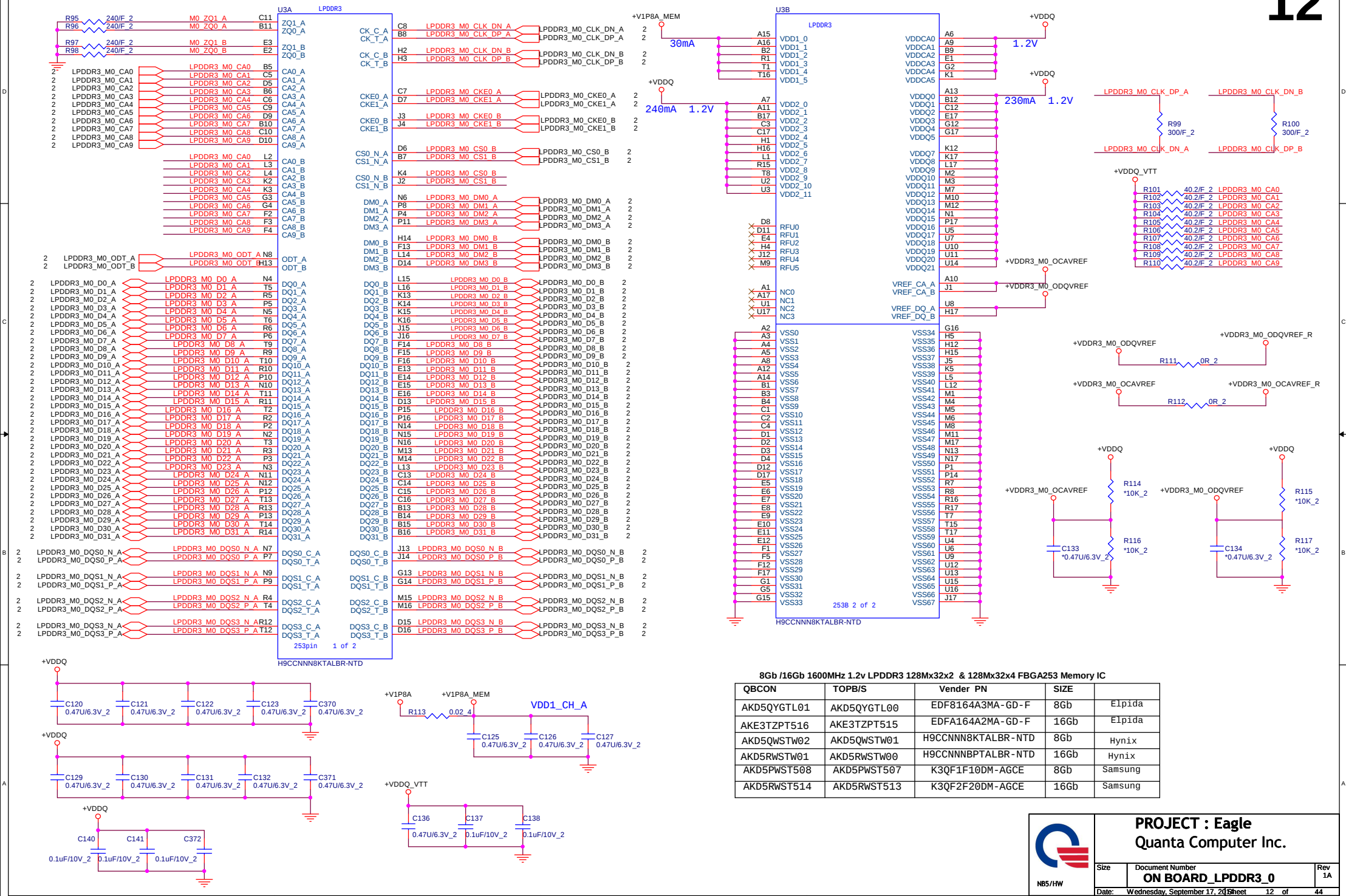
PROJECT : Eagle
Quanta Computer Inc.

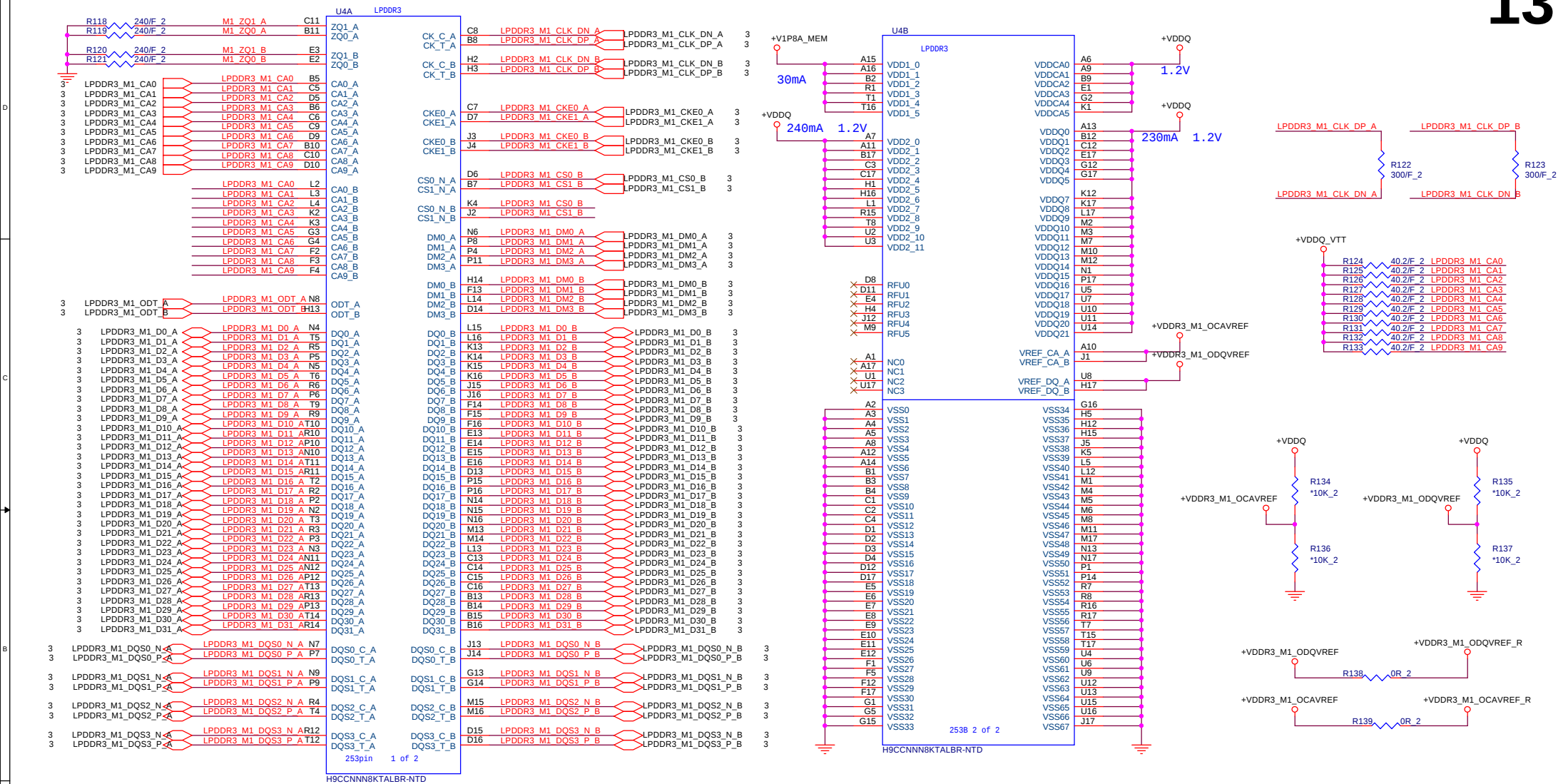
Size	Document Number	Rev
	Valleyview-T (GND)	1A
Date: Wednesday, September 17, 2014 Sheet 10 of 44		



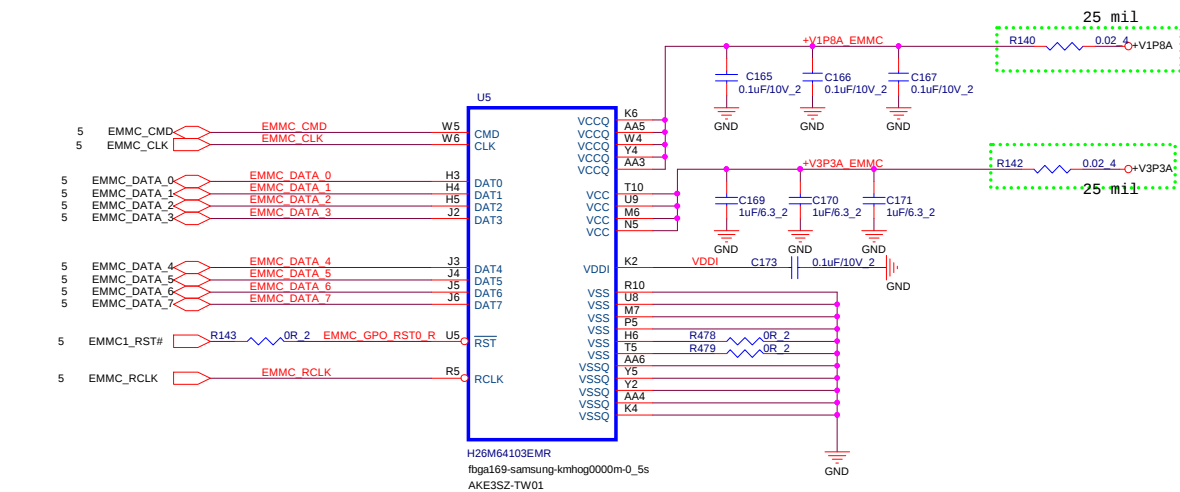
9,37,38	+V1P05A
8,9,24,37	+V1P15
8,9,12,13,37,38	+VDDQ
9	+V1P8A_SOC
9	+V3P3A_SOC
9,38	+V1P2A
7,9,38	+VRTC
9	+VCCSFR1ICKSI0_1P24_1P35
9	+VCCDSIPLL_1P24_1P35
9	+VCCTHMSOC_1P24_1P35
9	+VCCCPLLTHMCPU0_1P24_1P35
9	+VCCCPLLTHMCPU1_1P24_1P35
9	+VCCHGPLL_1P24_1P35

 NB5/HW	PROJECT : Eagle Quanta Computer Inc.	
	Size	Rev 1A
	Document Number Valleyview-T (GND)	
Date:	Wednesday, September 17, 2008	Sheet 11 of 44

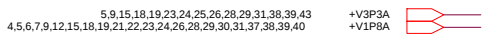
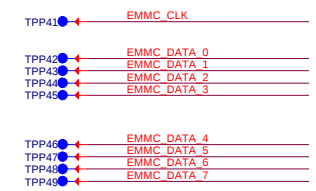




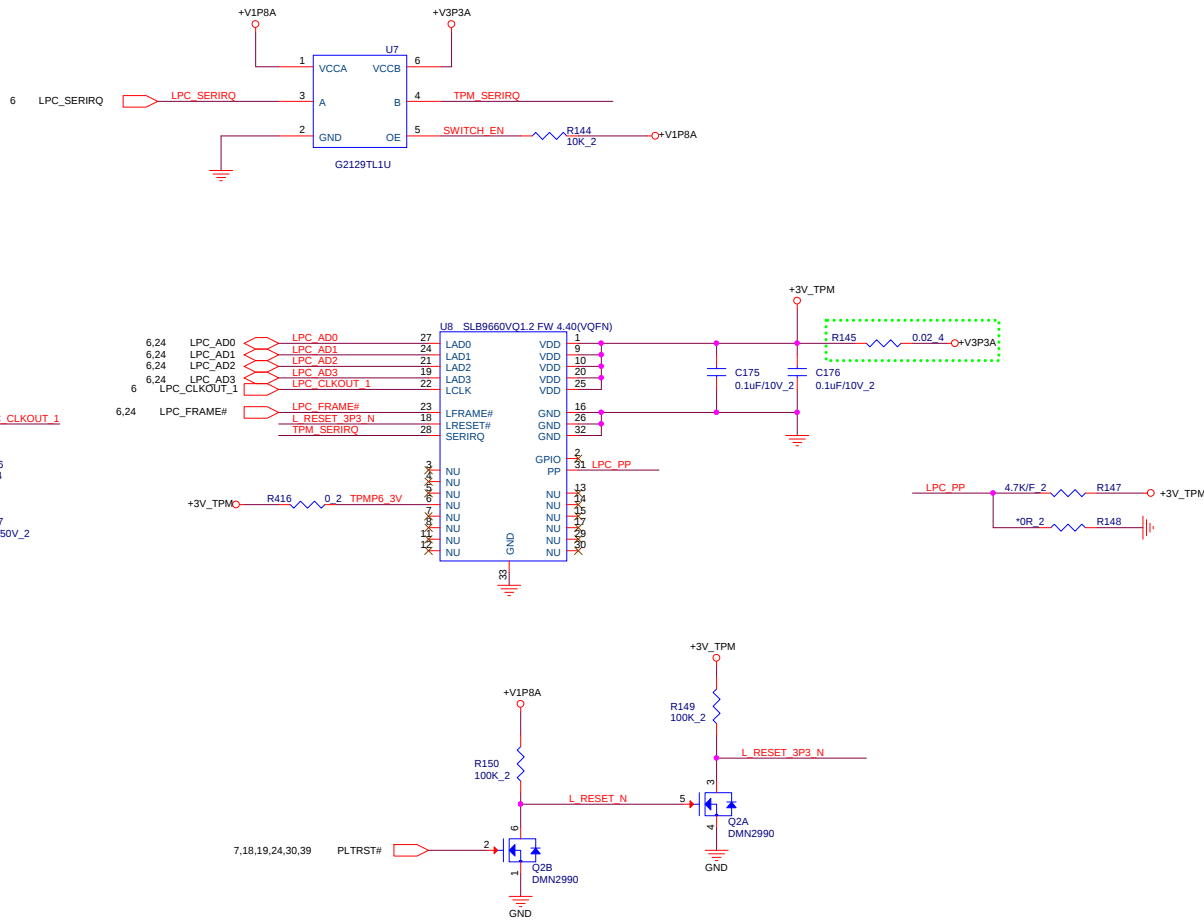
EMMC



footprint : BGA 169 \ BGA 153 co-lay
BGA 169 PIN : 14mmX18mm
BGA 169 PIN : 12mmX16mm
BGA 153 PIN : 11.5mmX13mm

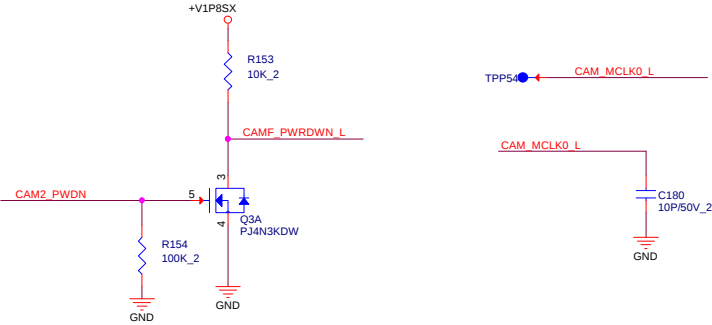
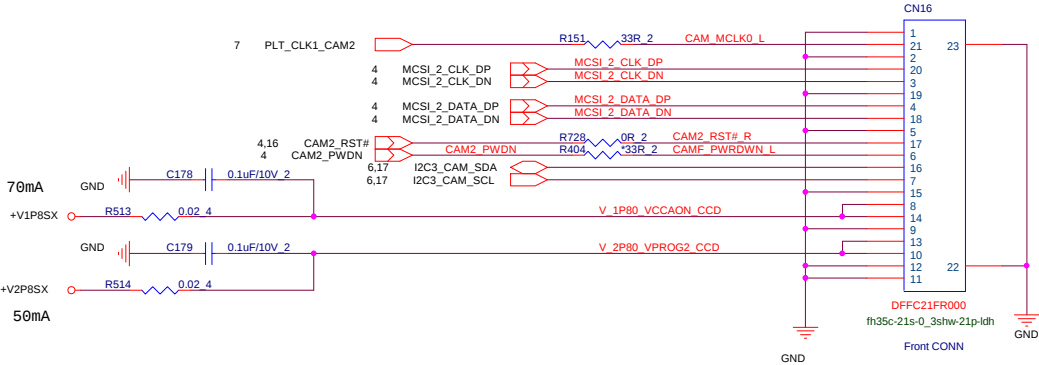


iNAND (eMMC 5.0)				
QBCON	TOPBIS	Vender PN	SIZE	
AKE5SZ0T507	AKE5SZ0T506	KLMBG4GEAC-B031	32G	Samsung
AKE3TZPT516	AKE3TZPT515	KLMBG8GEAC-B031	64G	Samsung
AKE3SZ-TW02	AKE3SZ-TW01	H26M64103EMR	32G	Hynix
AKE3TG-TW02	AKE3TG-TW01	H26M78103CCR	64G	Hynix
AKE3UFPT103	AKE3UFPT102	SDIN8CE4-128G	128G	Sandisk
AKE3SFUT001	AKE3SFUT000	SDIN9DW4-32G	32G	Sandisk
AKE3TFUT102	AKE3TFUT101	SDIN9DW4-64G	64G	Sandisk

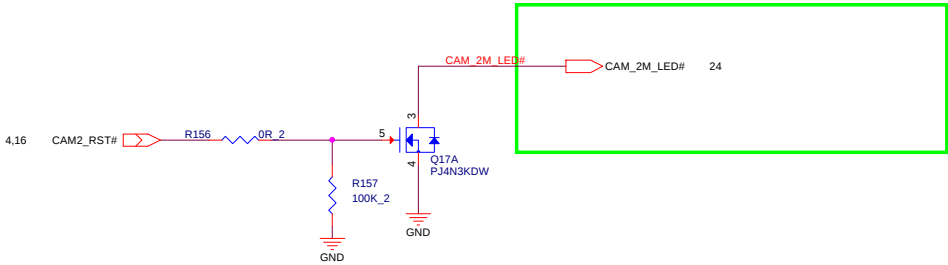


+V3P3A
+V1P8A

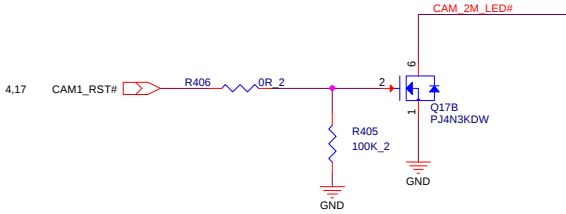
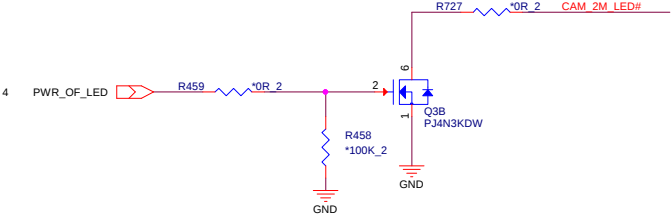
Front Camera Module Connector



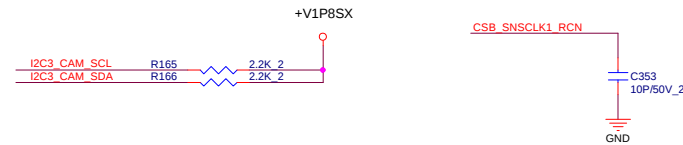
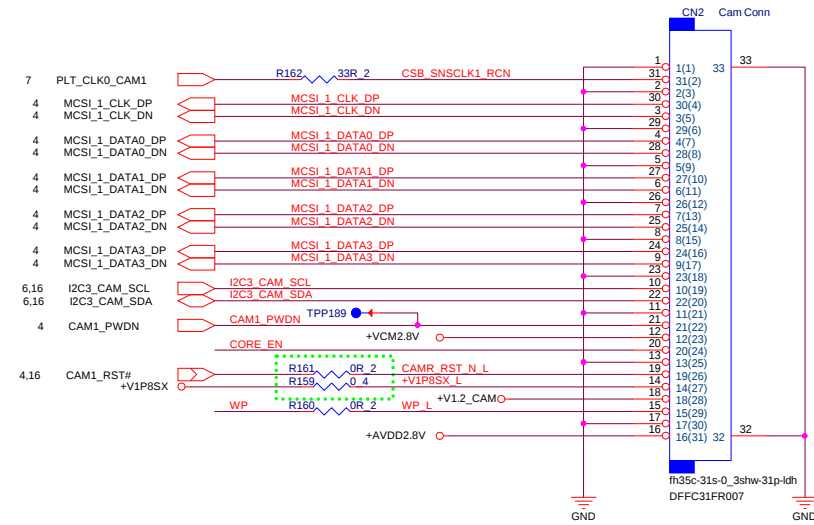
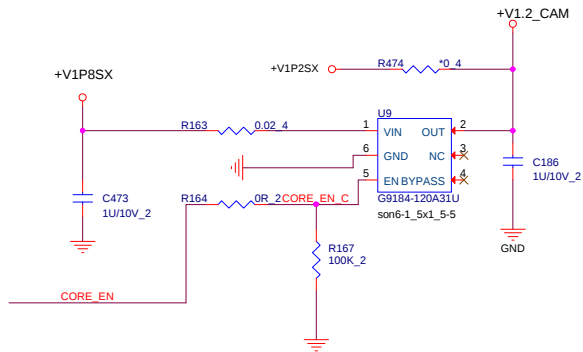
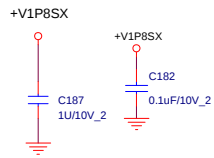
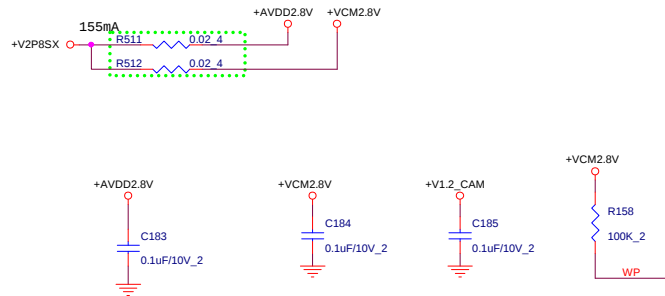
Camera 2M LED control



CAM_1_PWDN_L High --> power down



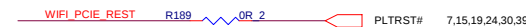
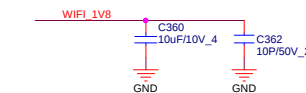
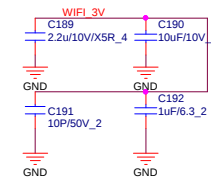
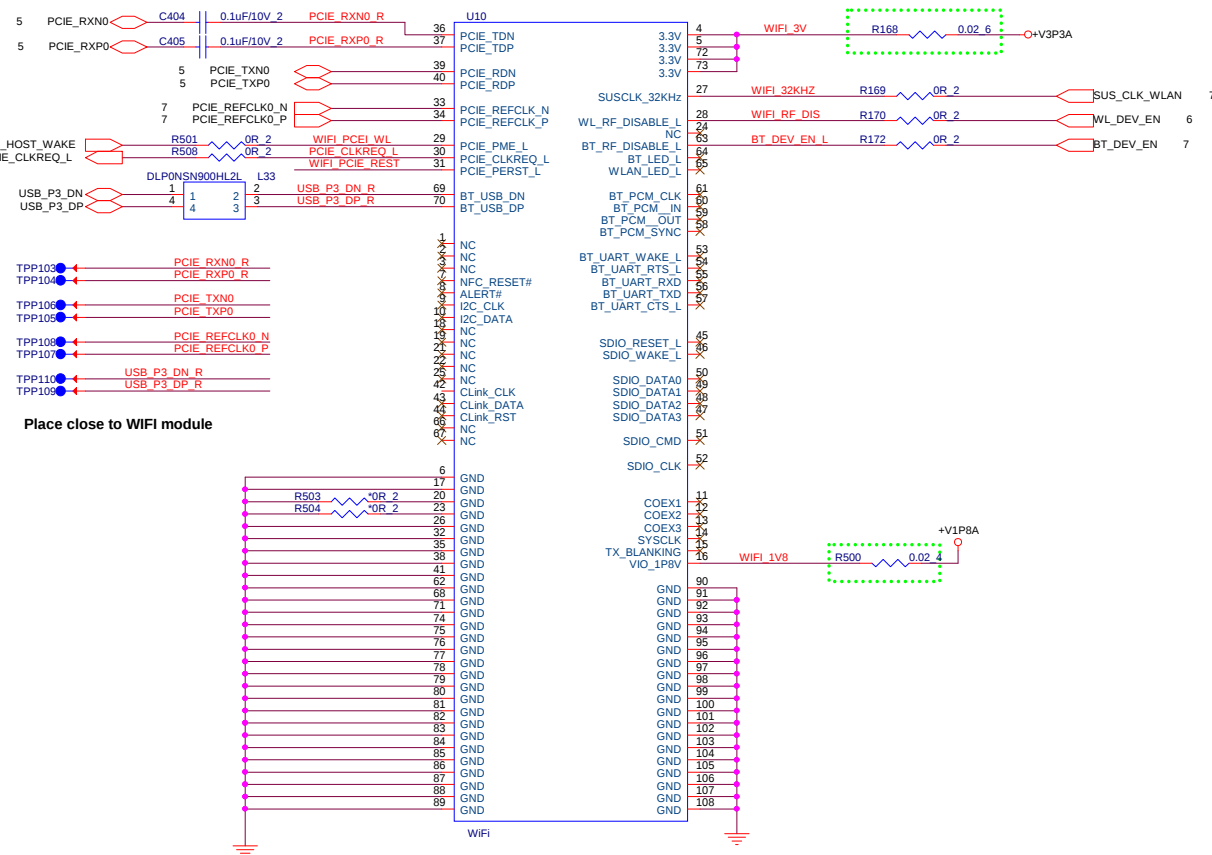
WEBCAM LED + CCD_8M CONNECTOR



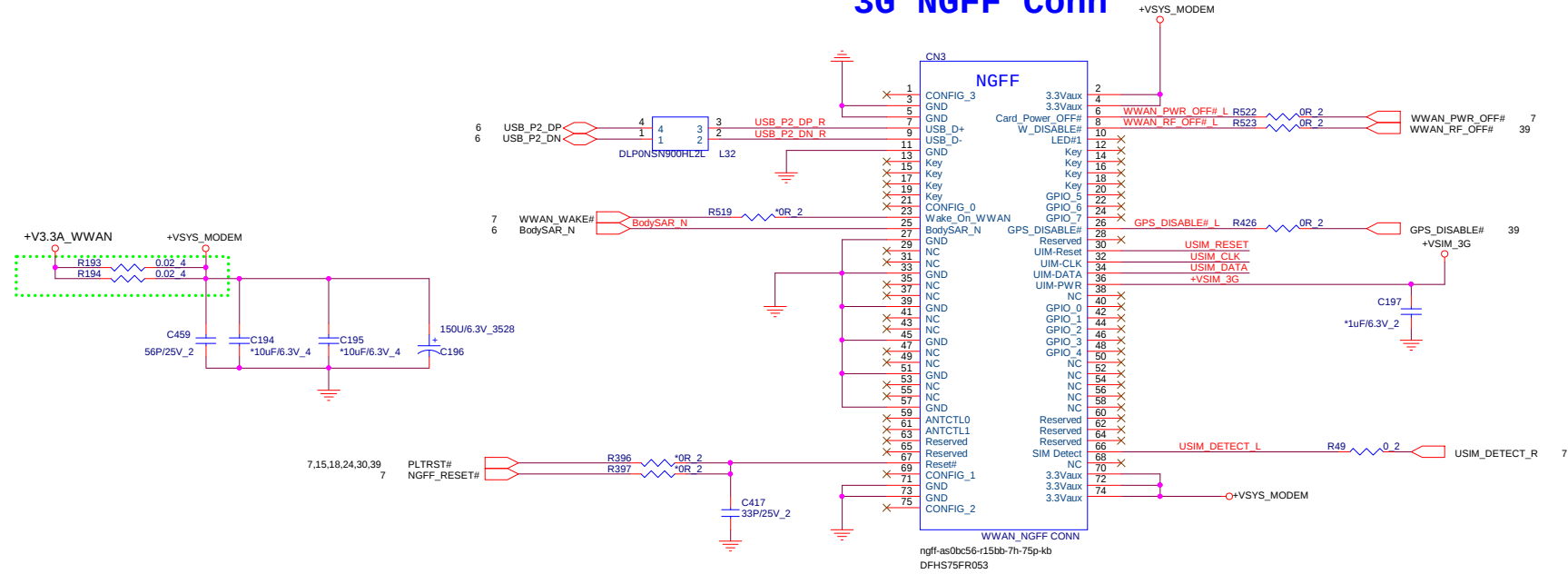
16,29,38 +V1P8SX
16,38 +V2P8SX
5,9,14,15,18,19,23,24,25,26,28,29,31,38,39,43 +V3P3A

5,9,14,15,19,23,24,25,26,28,29,31,38,39,43

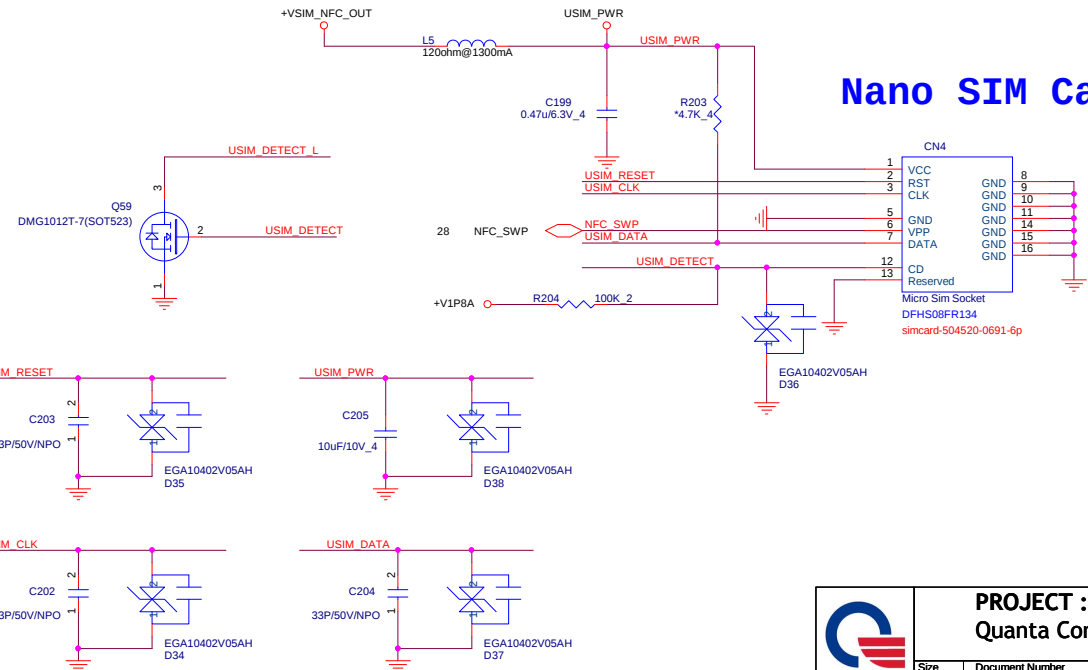
+V3P3A



3G NGFF Conn

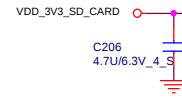


Nano SIM Card

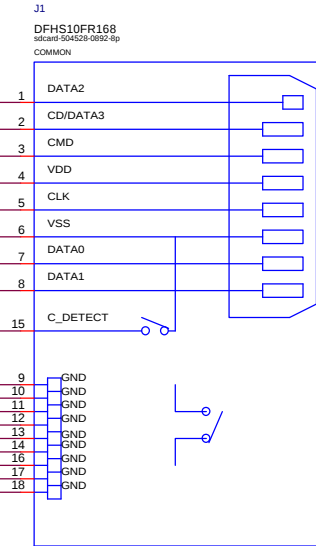


36 +V3.3A_WWAN
5,9,14,15,18,23,24,25,26,28,29,31,38,39,43 +V3P3A
4,5,6,7,9,12,14,15,18,21,22,23,24,26,28,29,30,31,37,38,39,40 +V1P8A

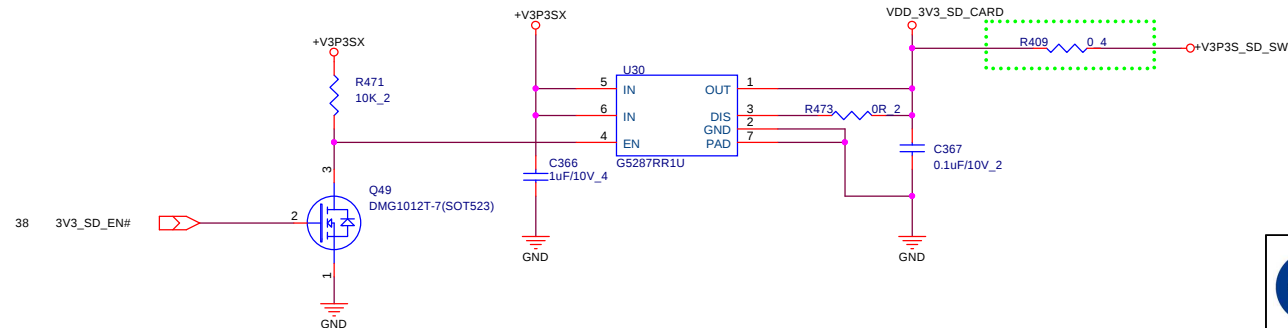
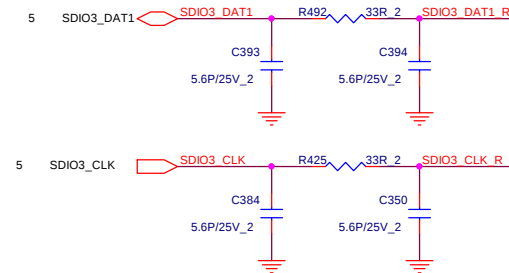
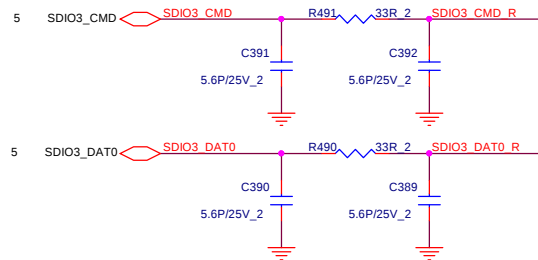
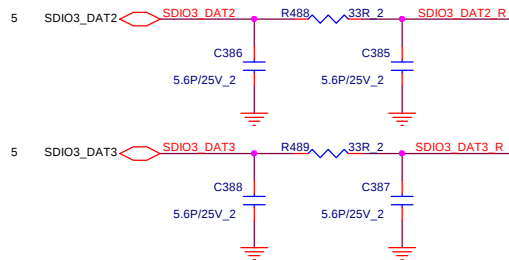
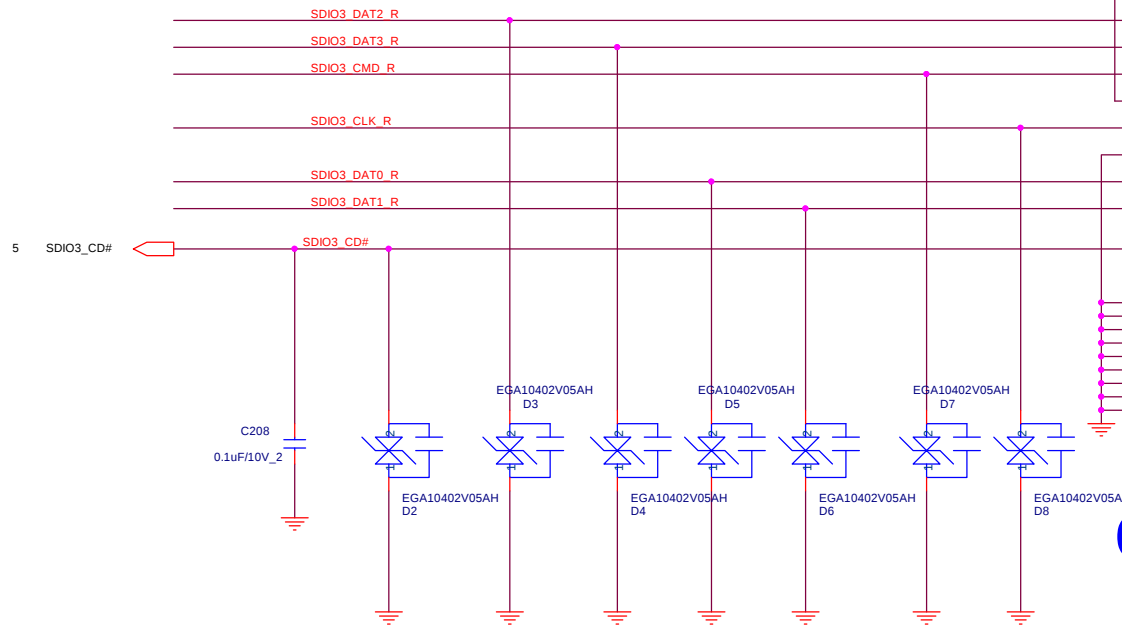
Place close to J3



microSD Card Socket



Card Reader

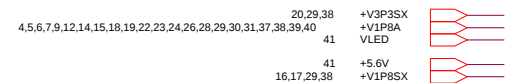
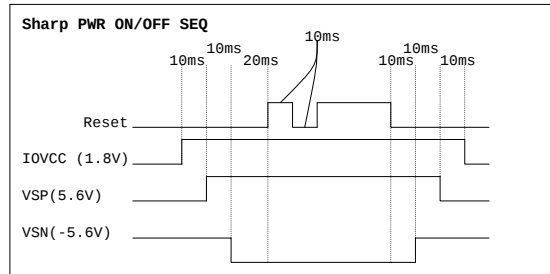
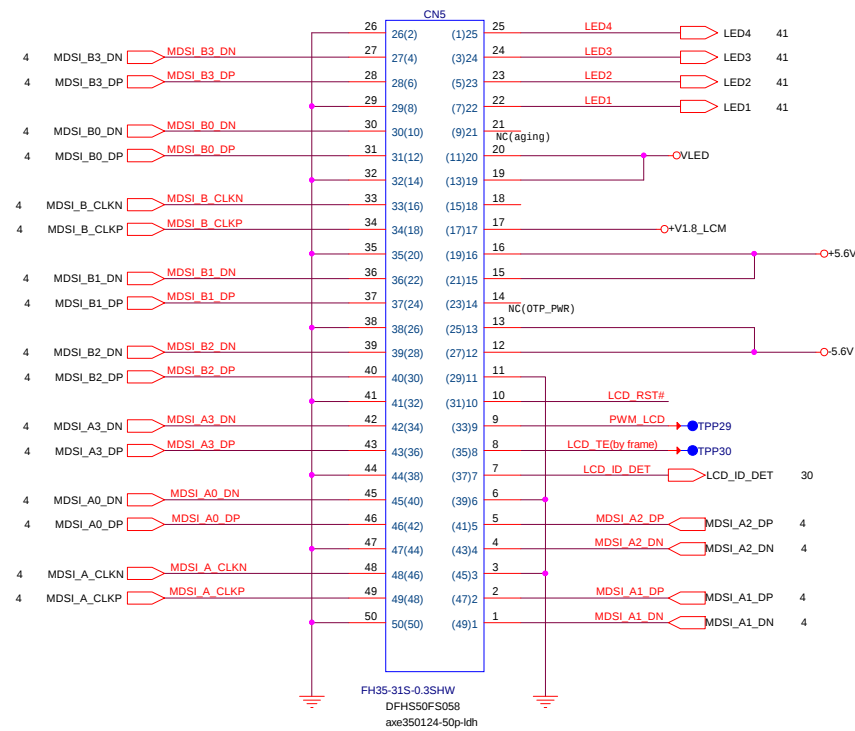
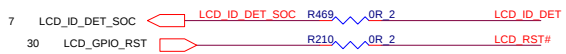
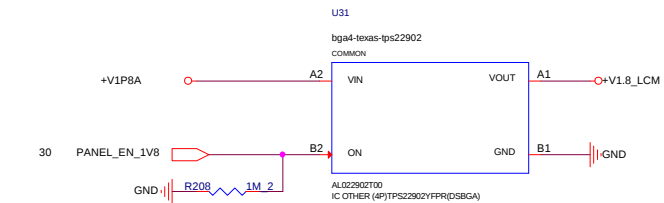
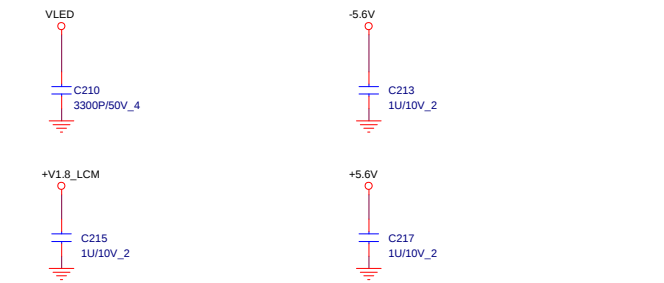


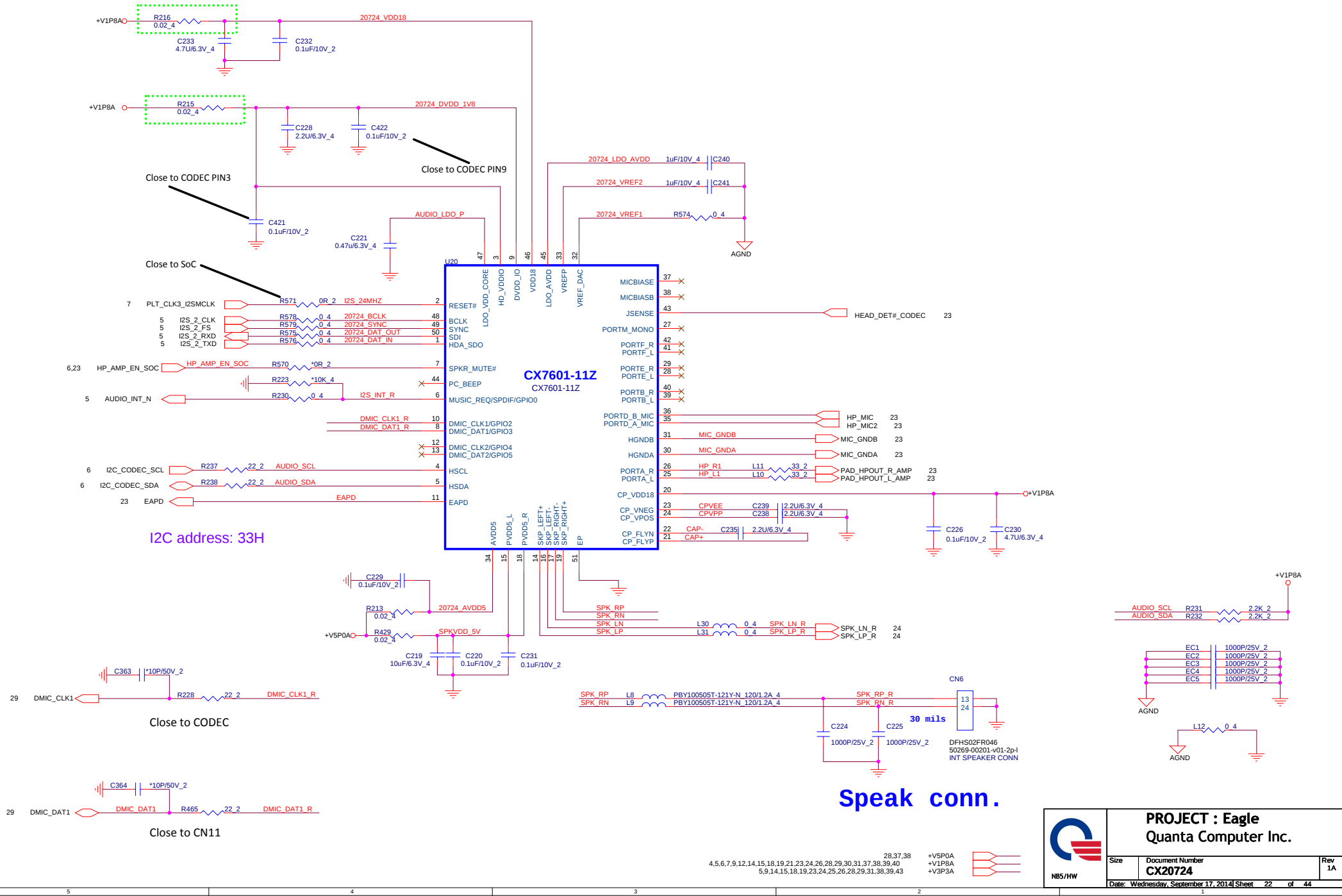
29,38 +V3P3SX
38 +V3P3S_SD_SW



**PROJECT : Eagle
Quanta Computer Inc.**

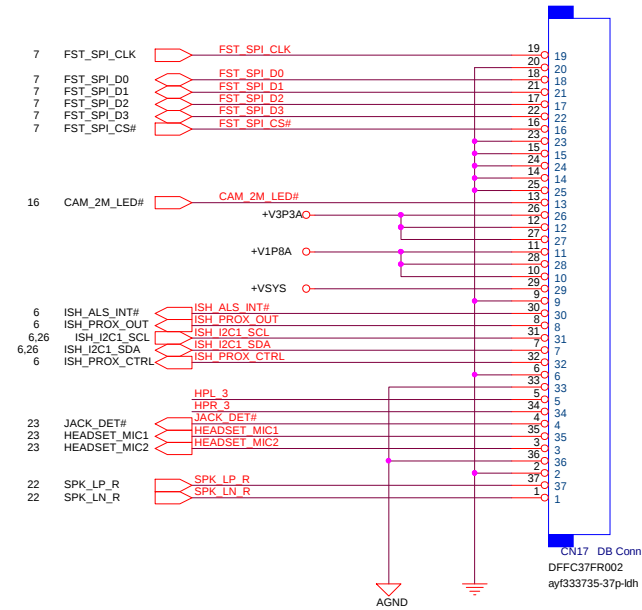
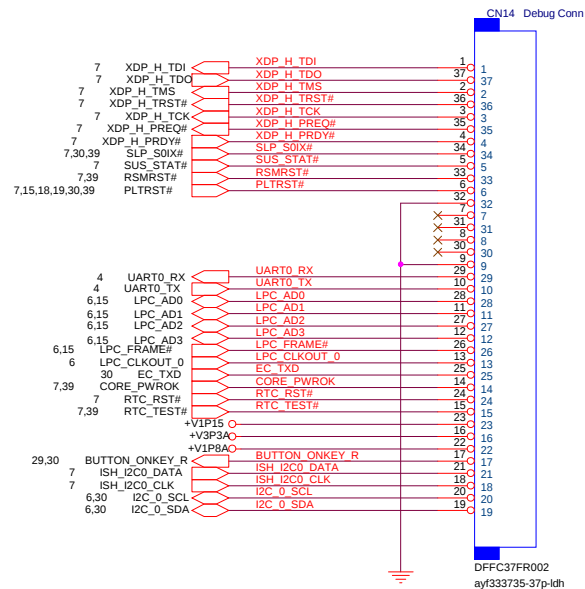
Size	Document Number	Rev
	MicroSD Card	1A
Date: Wednesday, September 17, 2014 Sheet 20 of 44		







SoC UART Debug



Microsoft Debug Switch

The diagram illustrates the Microsoft Debug Switch circuit, which interfaces the ICE UART pins with the target board's UART0 pins using two Texas Instruments TXS0101YZPR level shifters (U34 and U35).

U34 (TXS0101YZPR) Connections:

- VCCA:** Connected to +V1P8A.
- VCCB:** Connected to +V3P3A.
- A:** Connected to UART0_TX.
- B:** Connected to UART0_TX_3V3.
- OE:** Connected to 1V8_TXS0101 through a 100K resistor.
- Input Protection:** A 0.1uF/10V_2 capacitor (C381) is connected between A1 and B1 to ground.

U35 (TXS0101YZPR) Connections:

- VCCA:** Connected to +V1P8A.
- VCCB:** Connected to +V3P3A.
- A:** Connected to UART0_RX.
- B:** Connected to UART0_RX_3V3.
- OE:** Connected to 1V8_TXS0101.
- Input Protection:** A 0.1uF/10V_2 capacitor (C383) is connected between A1 and B1 to ground.

ICE UART Pins:

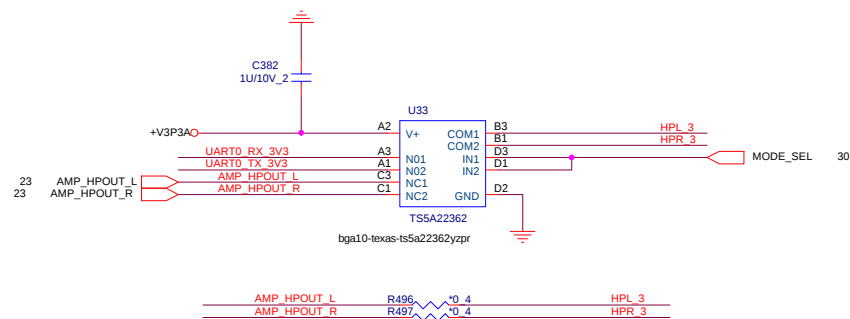
- ICE_UART_TX:** Connected to U34 pin A.
- ICE_UART_RX:** Connected to U35 pin A.

Target Board UART0 Pins:

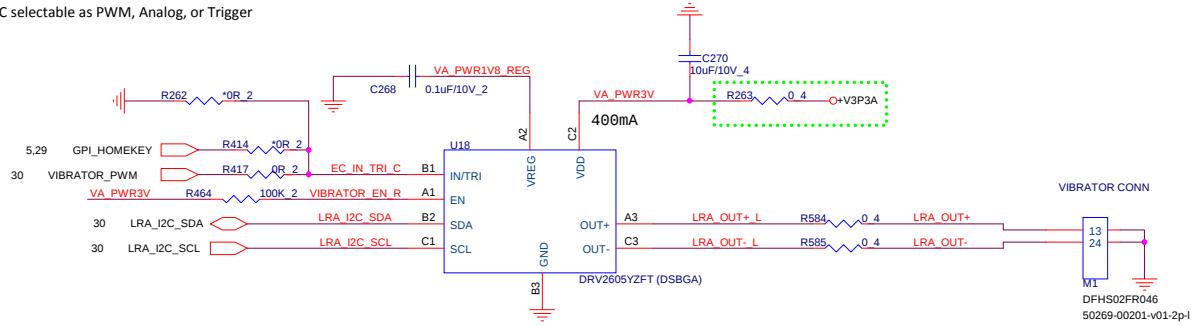
- UART0_TX:** Connected to U34 pin B.
- UART0_RX:** Connected to U35 pin B.

Power and Grounding:

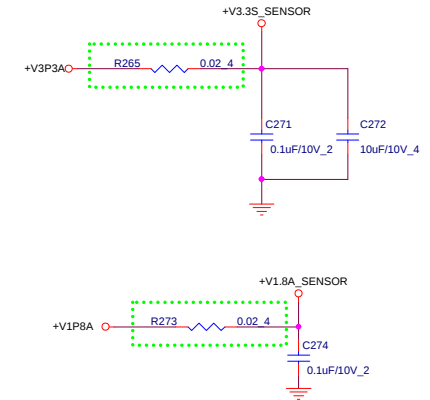
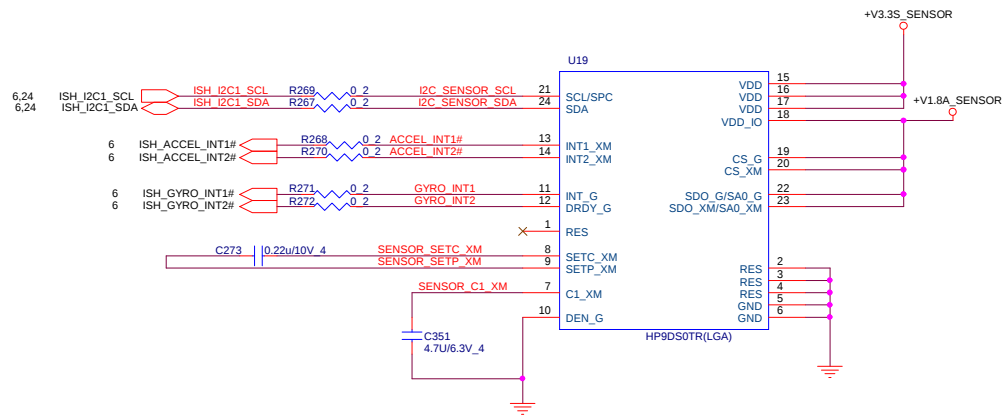
- +V1P8A:** Provides 1.8V supply to both level shifters.
- +V3P3A:** Provides 3.3V supply to both level shifters.
- 1V8_TXS0101:** Provides 1.8V supply to the OE pins of both level shifters.
- Resistors:** R696 (0.2 ohms) and R697 (0.2 ohms) are connected in series with the ICE UART_TX and ICE_UART_RX pins, respectively.
- Capacitors:** C381 and C383 (0.1uF/10V_2) are connected between the input pins (A1/B1) and ground for input protection.



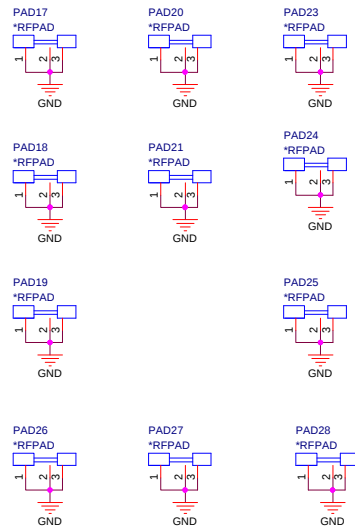
Multi-mode Input. I2C selectable as PWM, Analog, or Trigger



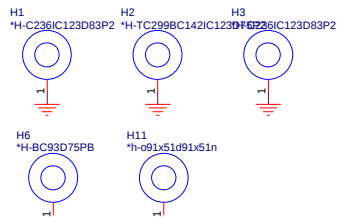
3D accelerometer, 3D gyroscope, 3D magnetometer



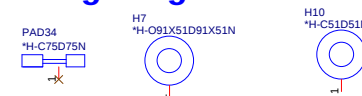
Top Shielding Can using



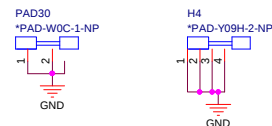
Hole



Aligning hole



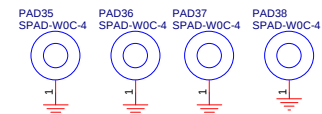
BOT SHIELDING PAD



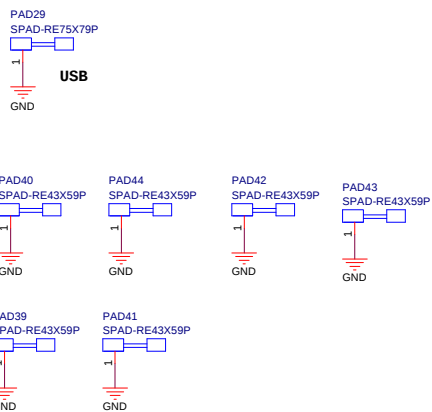
TOP SHIELDING PAD



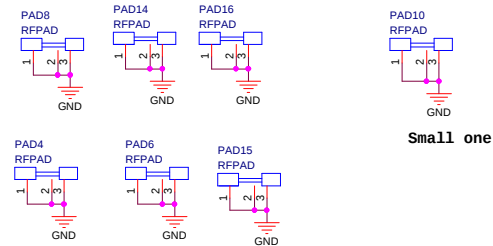
Nut



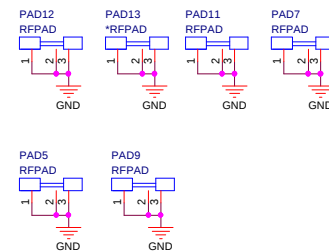
ME WIRE PAD



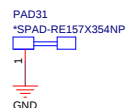
BOT shielding: Up



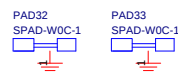
BOT shielding: Down

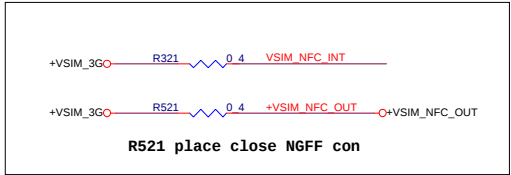
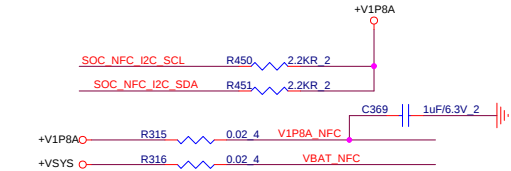
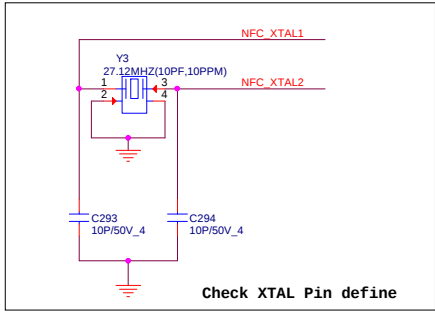


TS GND PAD



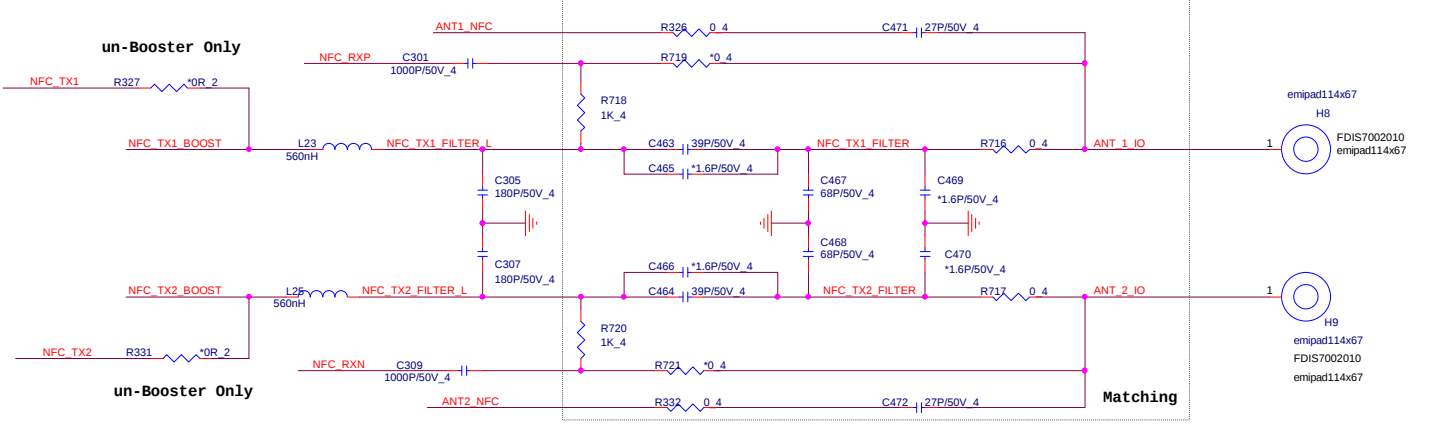
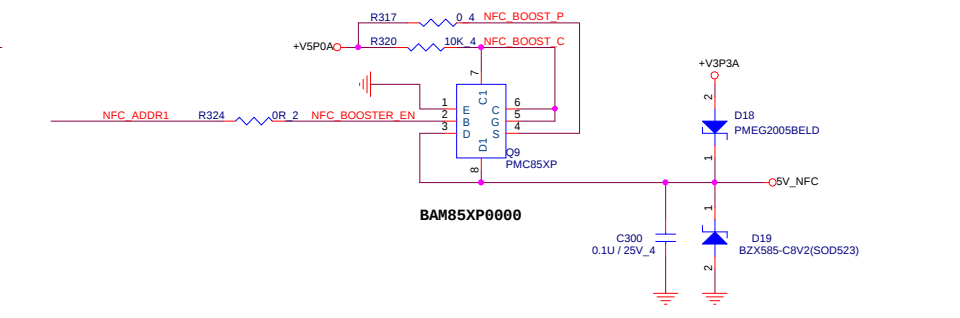
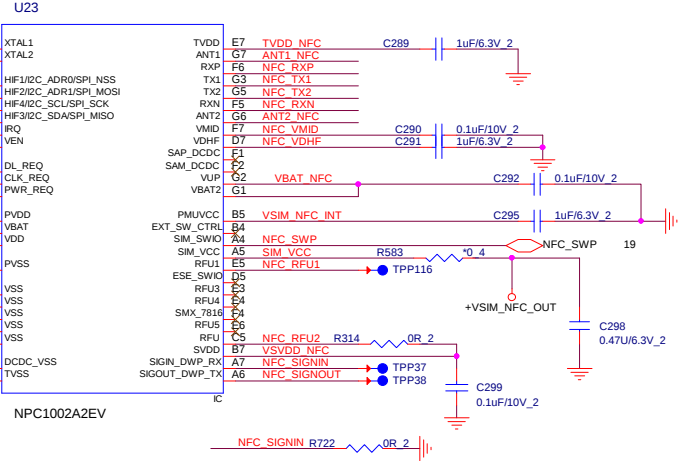
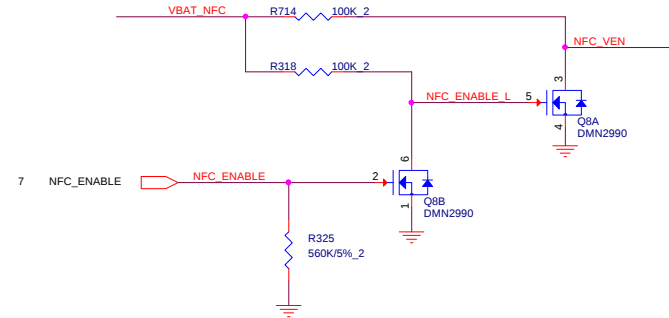
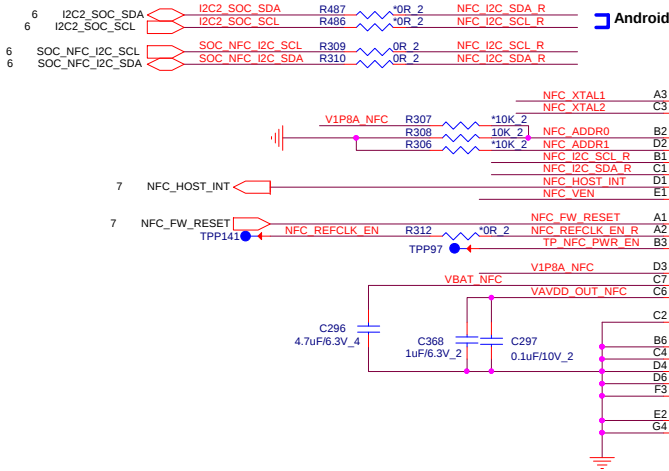
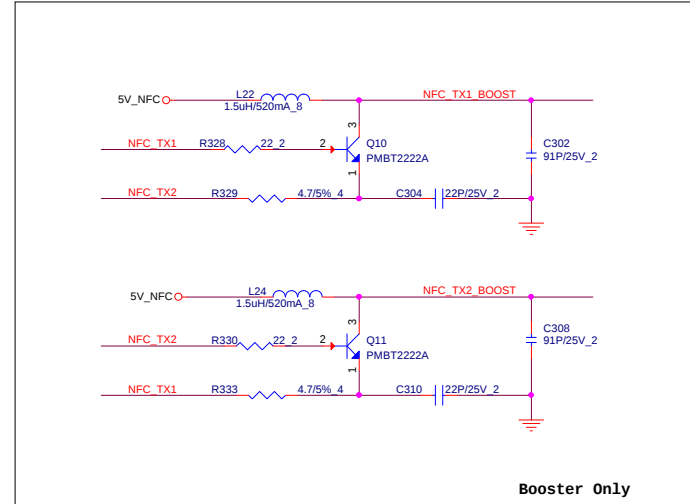
USB3 SHIELDING

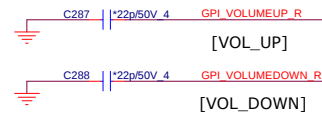
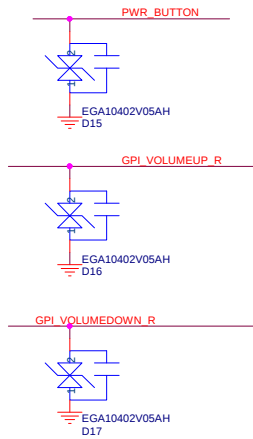
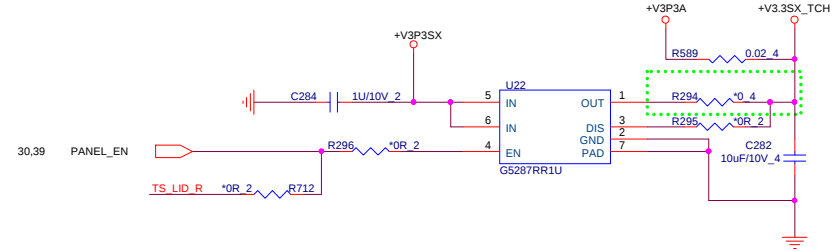
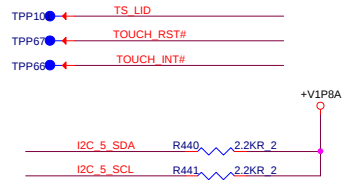
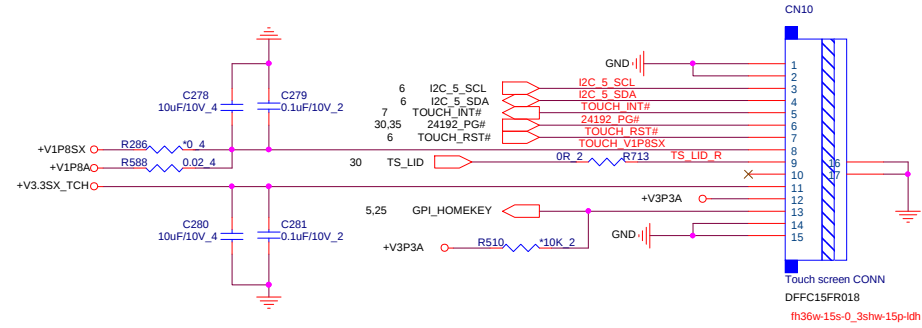




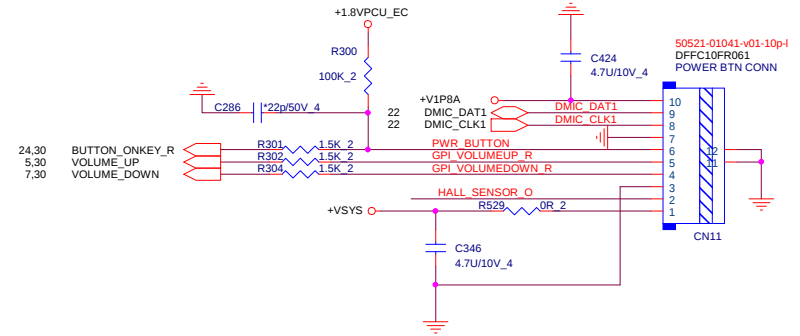
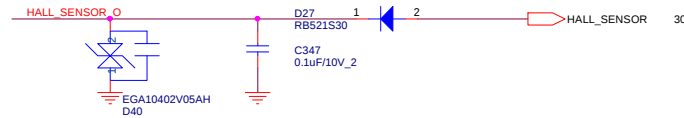
4,5,6,7,9,12,14,15,18,19,21,22,23,24,26,29,30,31,37,38,39,40
5,9,14,15,18,19,23,24,26,29,31,38,39,43

+V1P8A
+V3P3A

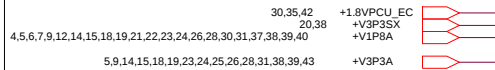


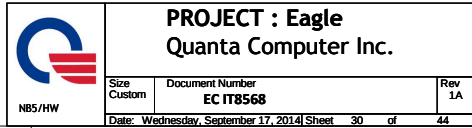


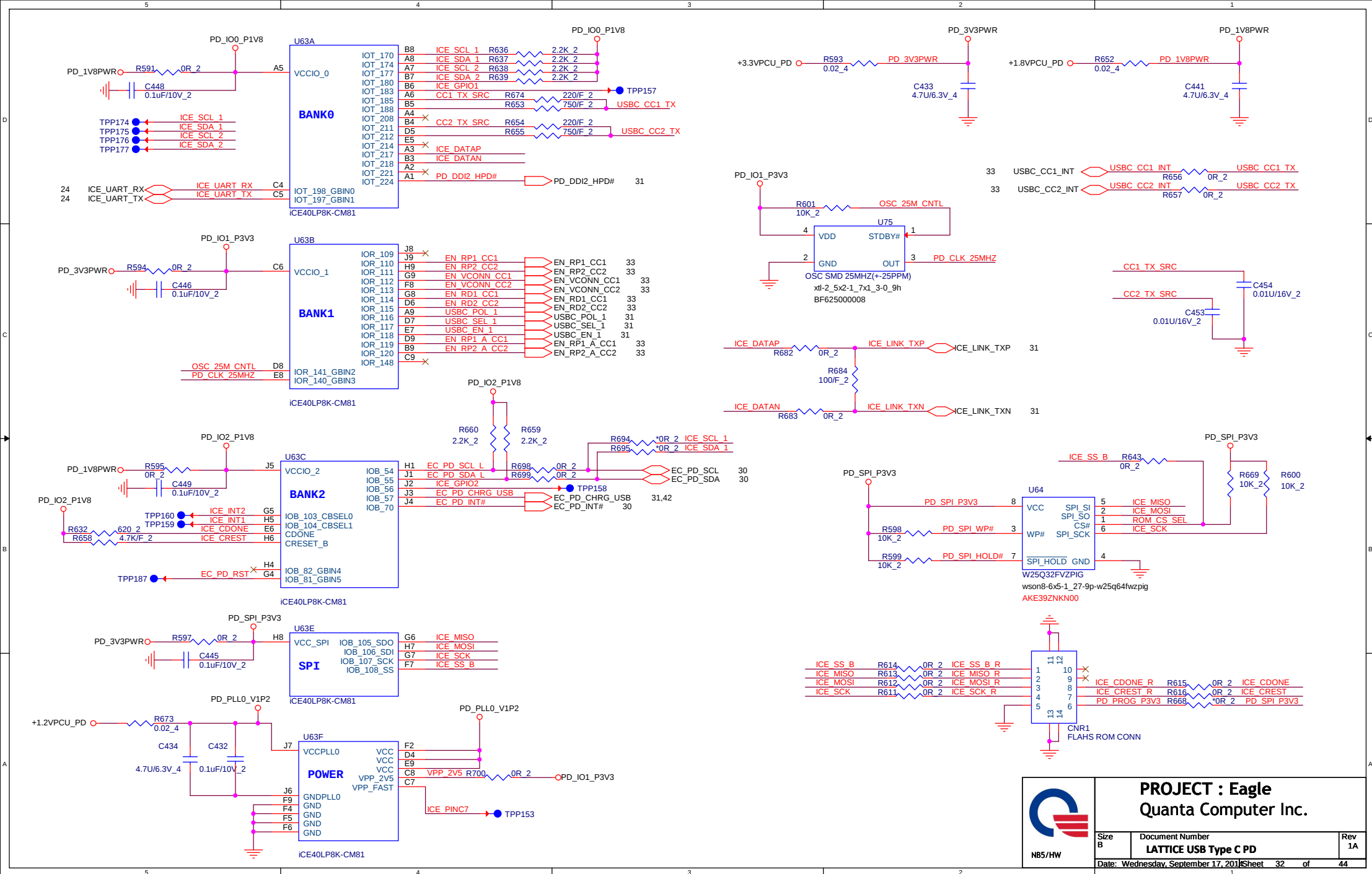
Hall Sensor

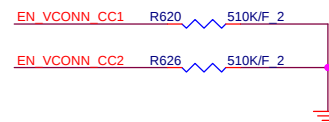
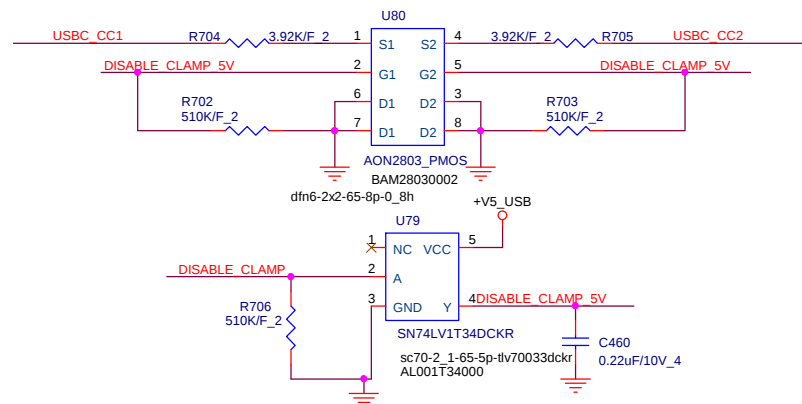
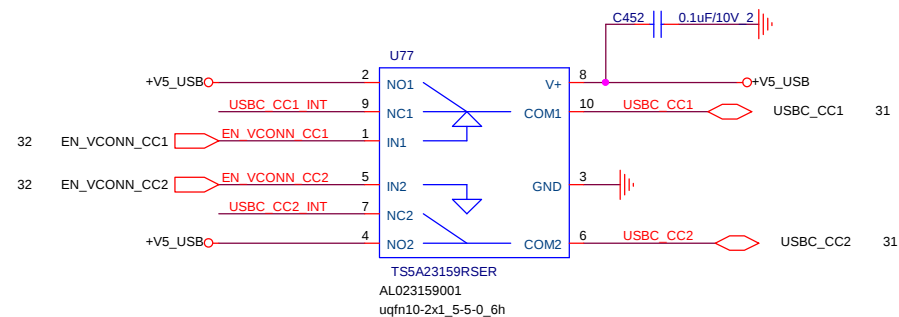
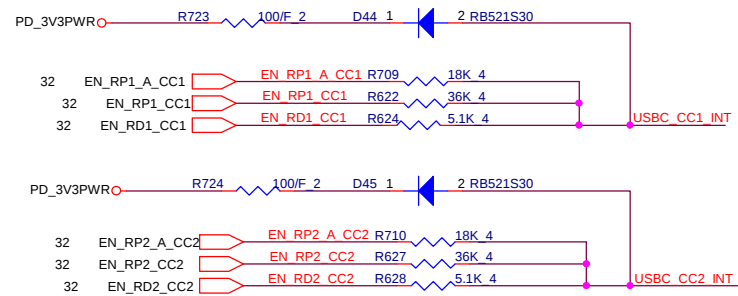
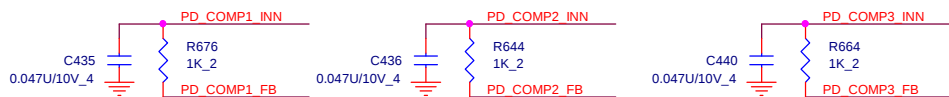
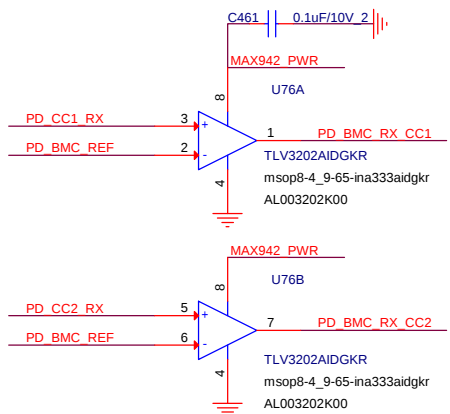
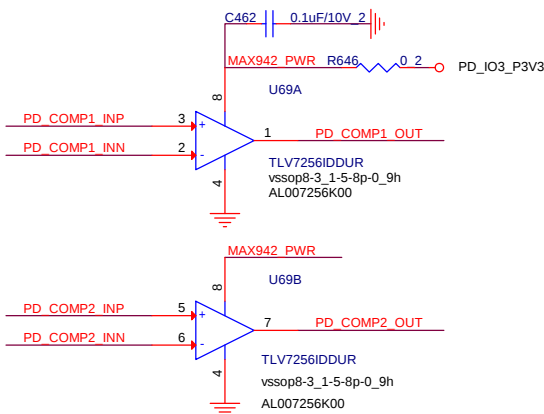
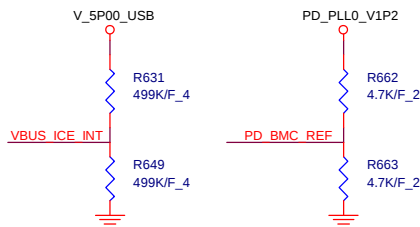
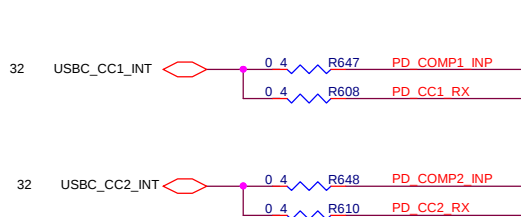
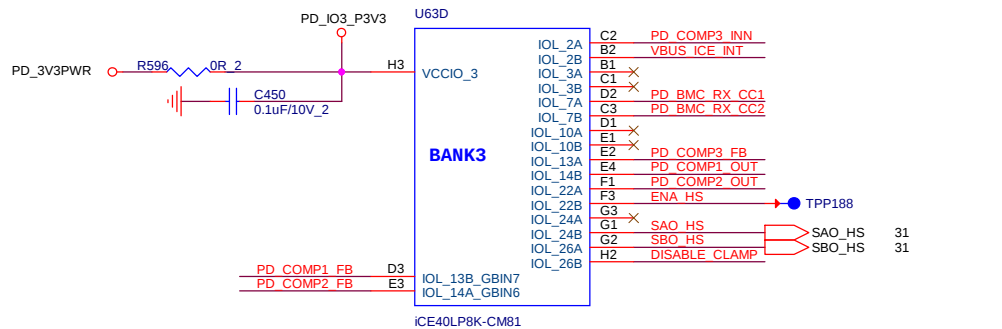


PWR & Vol Conn









		
Size B	Document Number	Rev 1A
LATTICE USB Type C PD		
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SoC I2C	Function	Address	Speed
0	EC	ACPI / WMI : 0x76 (7bit) 0xEC (8bit) Flash : 0x5B (7bit) 0xB6 (8bit)	400k Hz
1	Audio	33h	400k Hz
3	Camera	8M-->IMX219 0x20/0x21 (8bit) 2m-->OV2724 SiD=0, 0x6C (8bit)	400k Hz
4	HDMI	NA	NA
5	Touch Screen	0X4B	400k Hz
6	PMIC	0x5E (8bit) 0x6E (8bit)	HS mode (3.4 MHz)
7 (NFC)	NFC	ADR:0 & ADR1: 1 W:0x54 ; R: 0x55 (8bit)	HS mode (3.4 MHz)
ISH	Combo Sensor	acceleration and magnetic (8bit) Read 0x3B Write 0x3A Angular--> Read 0xD7 Write 0xD6	400k Hz
ISH	ALS	Ra PD: 0x10 (default) Ra PU: 0x48	400k Hz
ISH	SAR	0 x 28 (Check table 8) (7bit)	400k Hz

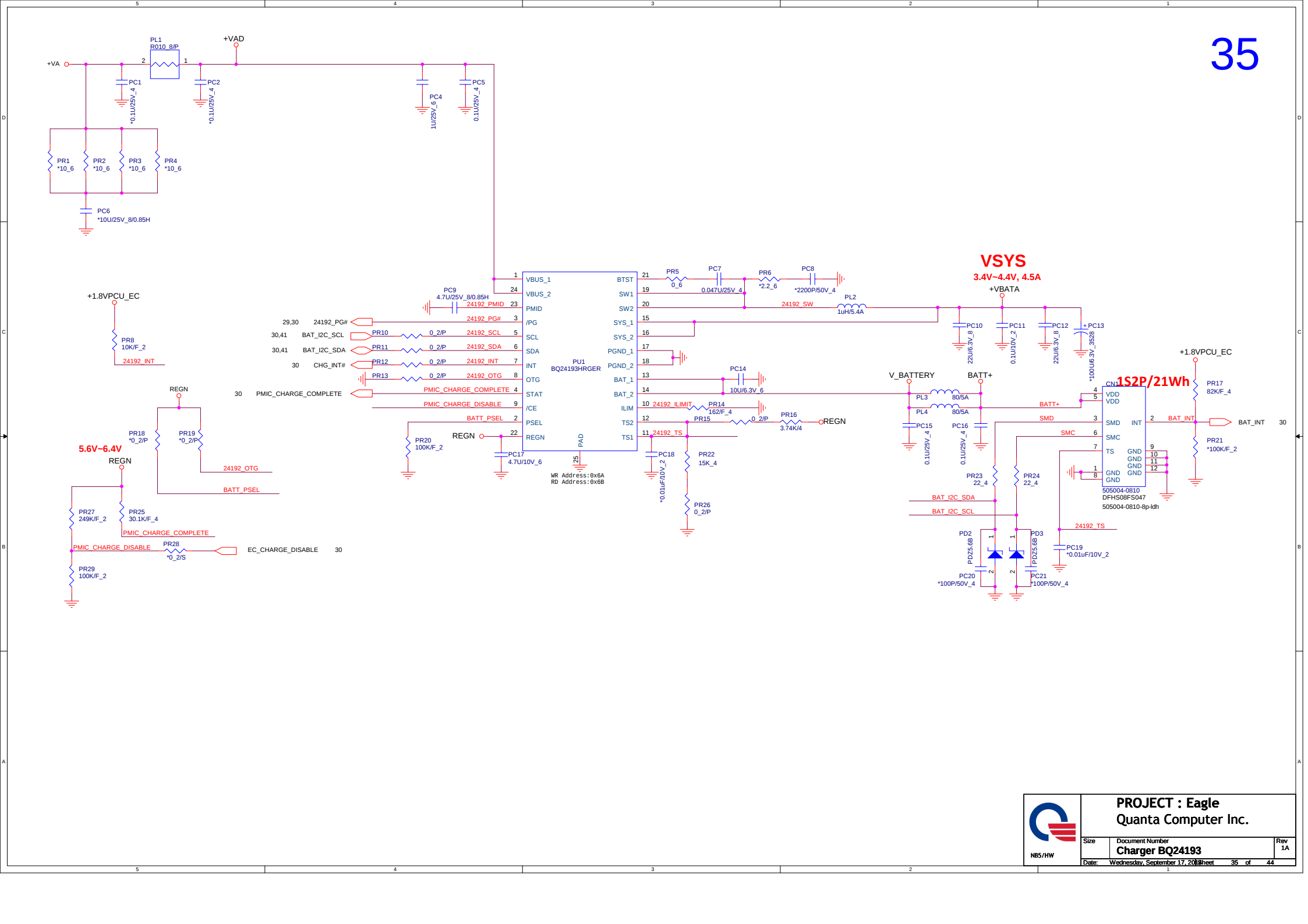
EC I2C	Function	Address	Speed
0	SoC		HS-mode
2	TPS65132	W: 0x7C R: 0x7D (8bit)	
	Battery		
	Charger	W: 0x6A R: 0x6B (8bit)	400k Hz
3	POGO		
1	PD		
	DOCK		
	Moto Driver	W:0xB4 R: 0xB5 (8bit)	400k Hz

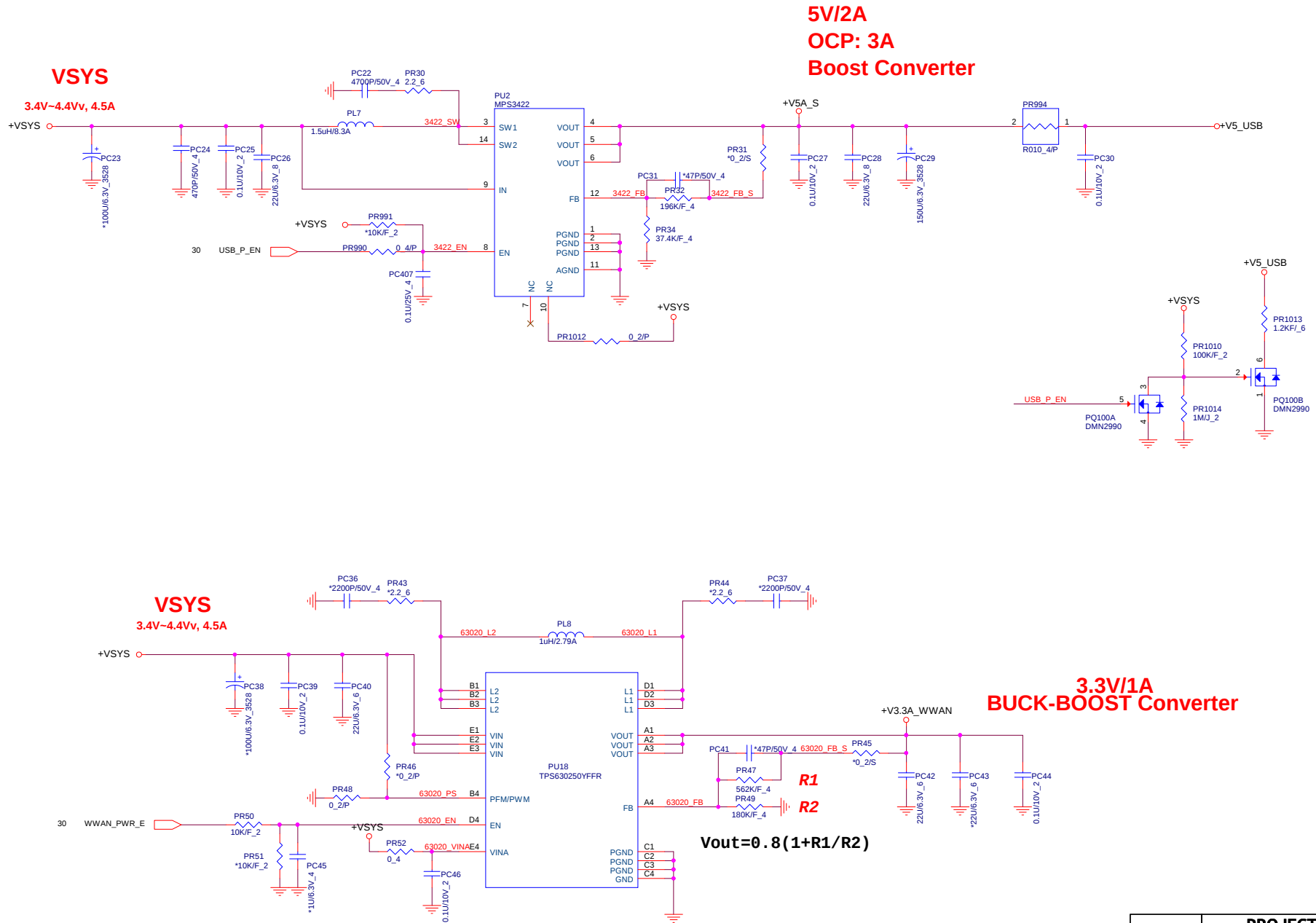
Table 15. I²C-bus interface addressing

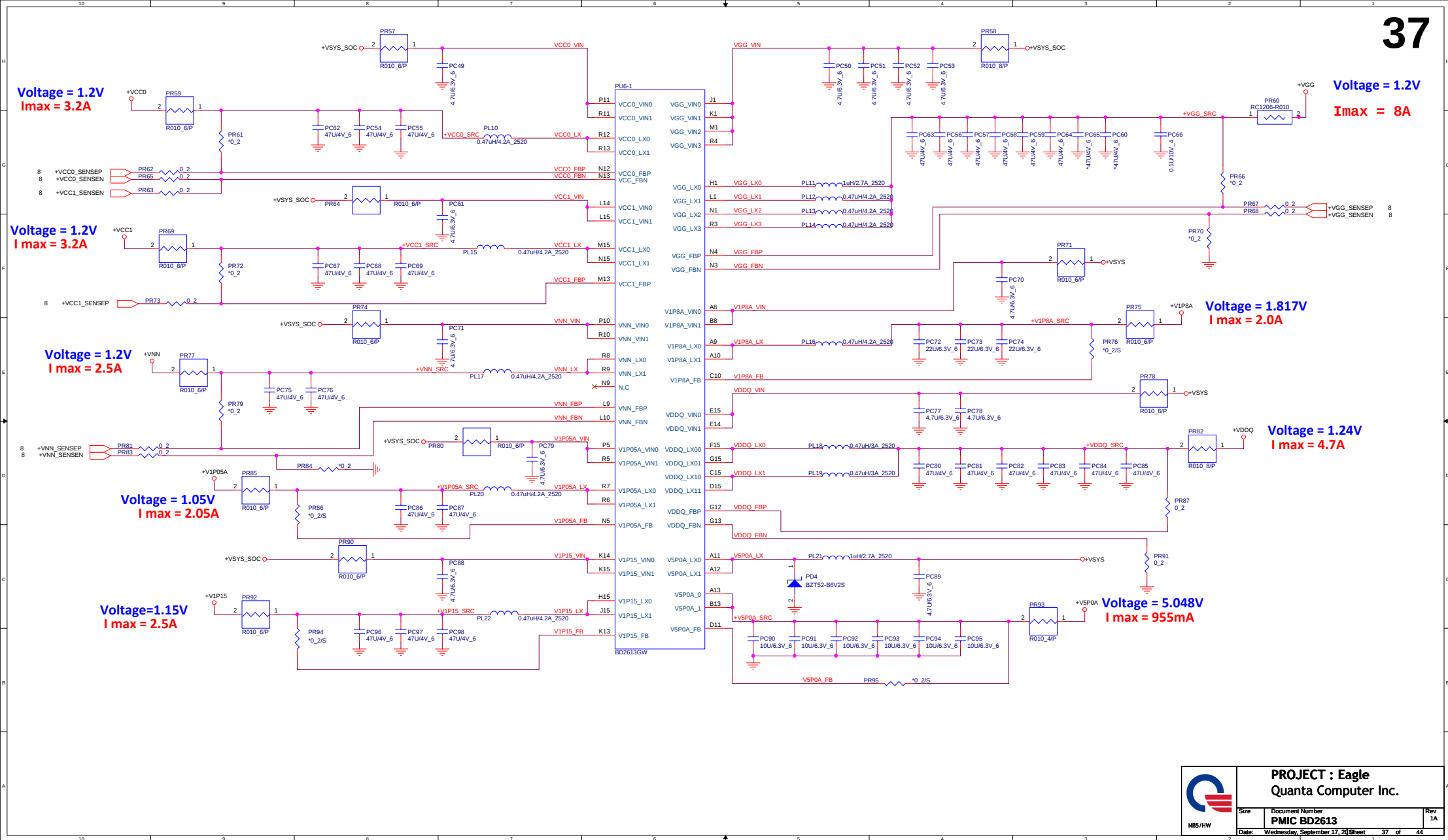
I2C_ADR1	I2C_ADR0	I ² C-bus address (R/W = 0, write)	I ² C-bus address (R/W = 1, read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

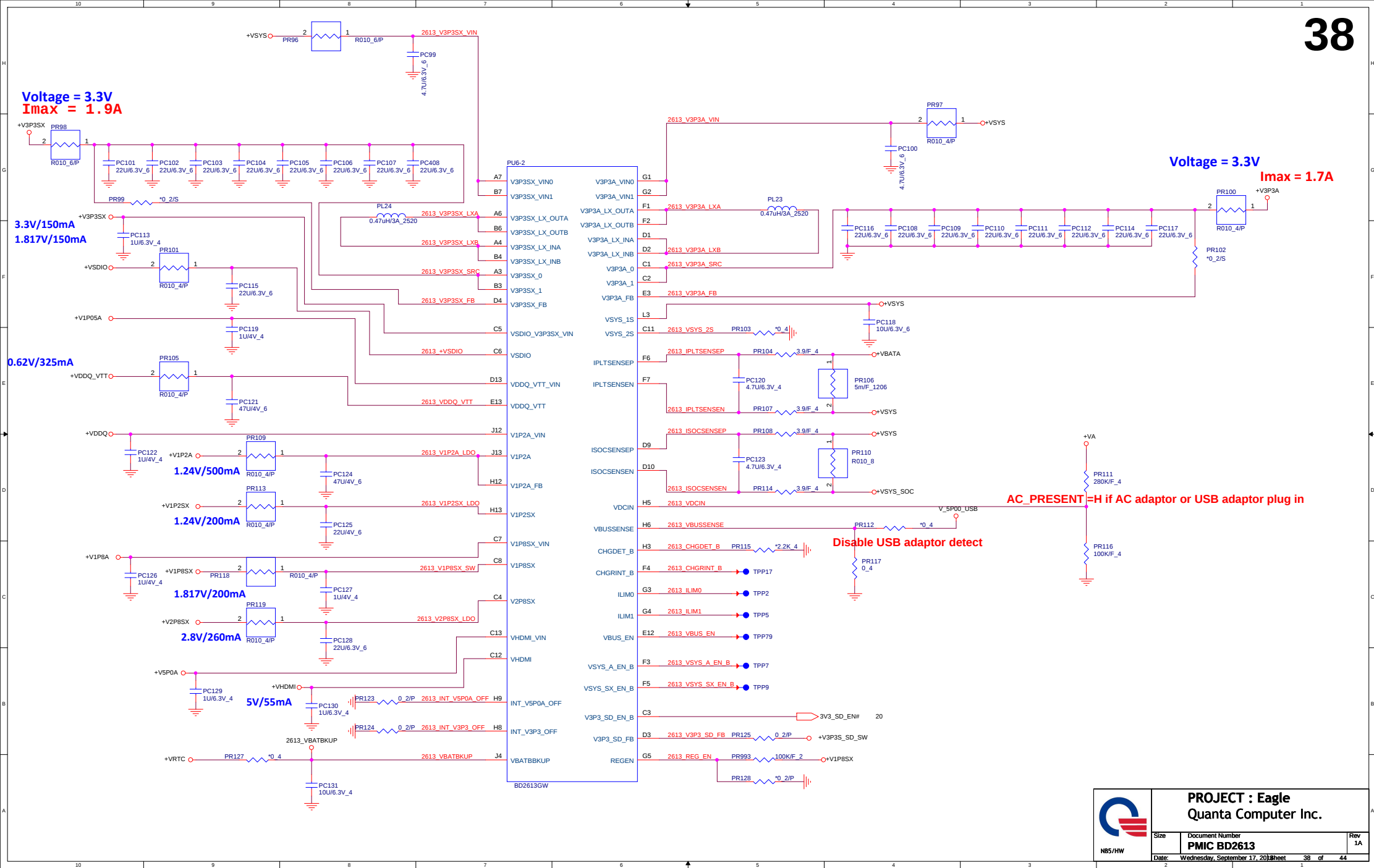
A1	A0	Address
0	0	0x28
0	1	0x29
1	0	0x2A
1	1	0x2B

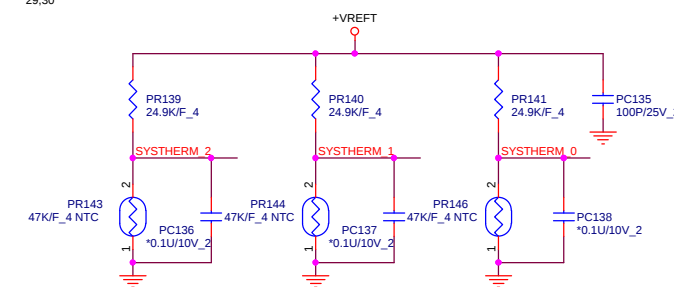
Table 8: I2C Sub-Address Selection





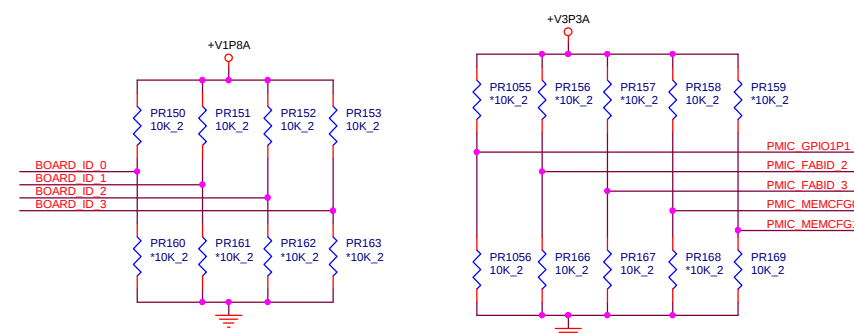


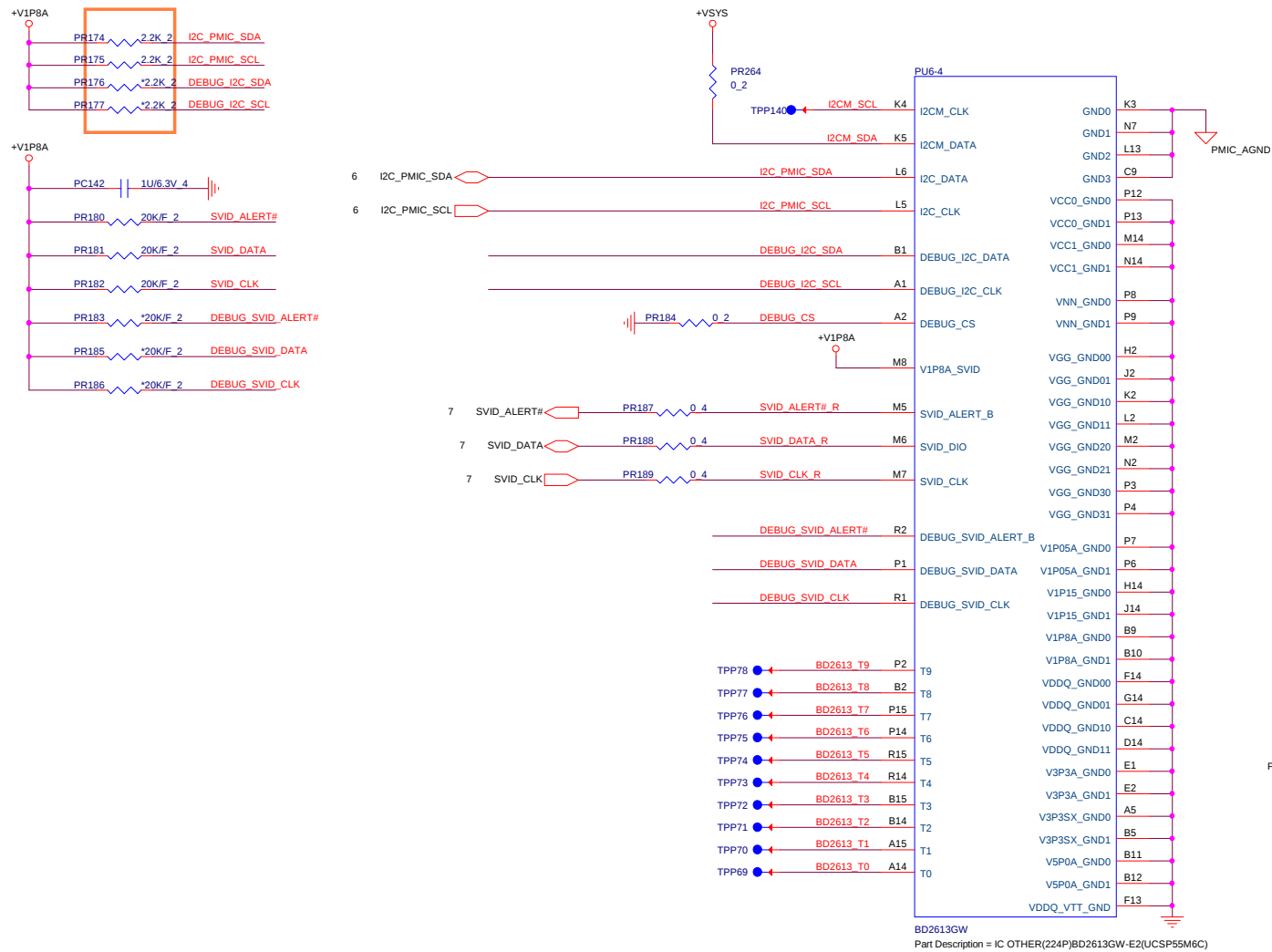




VDDQ_SET	LPDDR3	DDR3L
	GND	VSYS

Board ID	ID 2	ID 3	SKU	ID 1	ID 0
DB	1	1	WO-WAN ; WO-NFC	0	0
SI 1	0	1	WO-WAN ; W-NFC	0	1
SI 2	1	0	W-WAN ; WO-NFC	1	0
PV / MV	0	0	W- WAN ; W-NFC	1	1

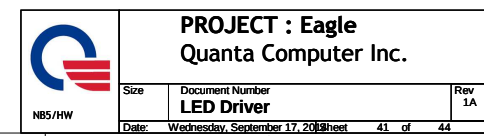


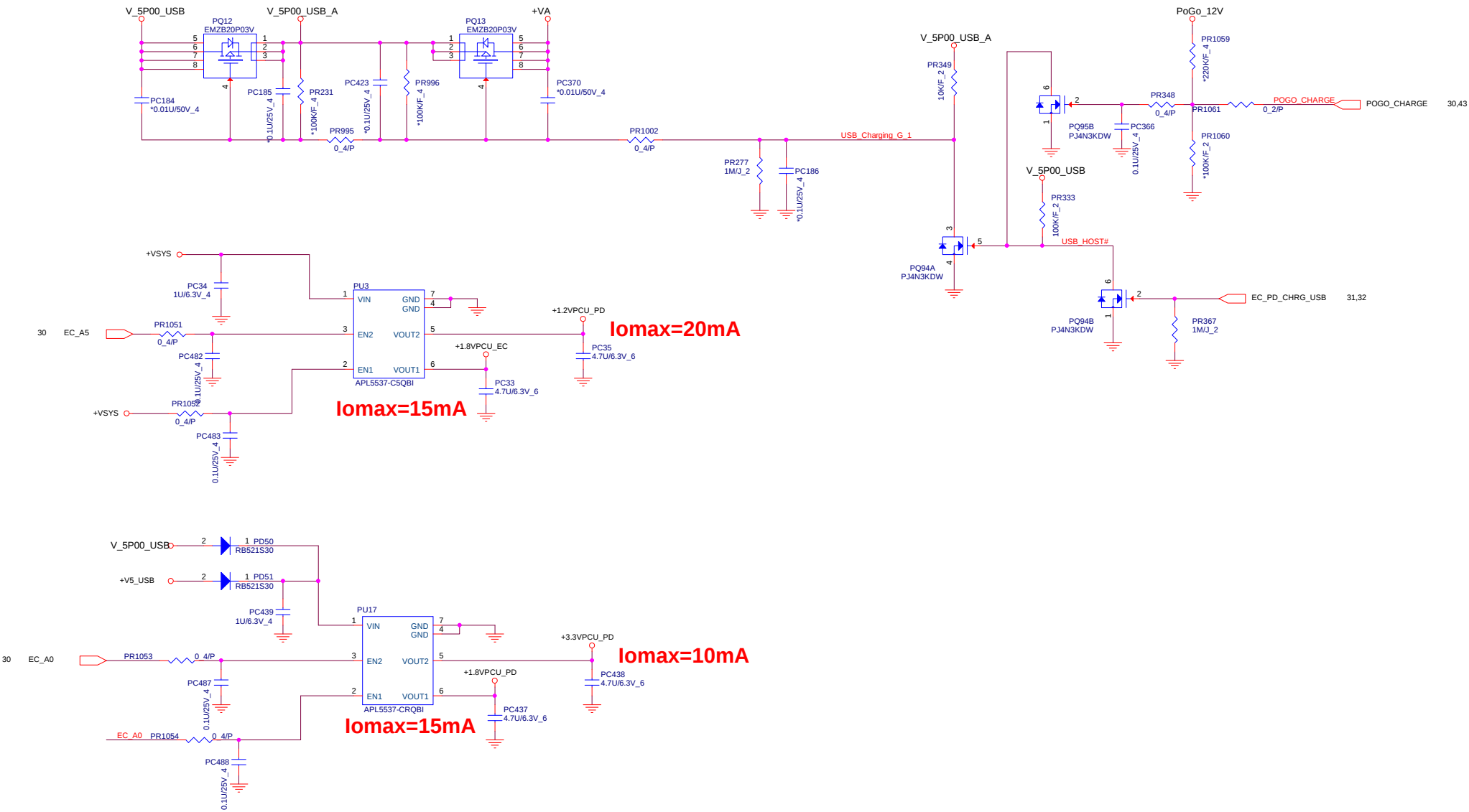


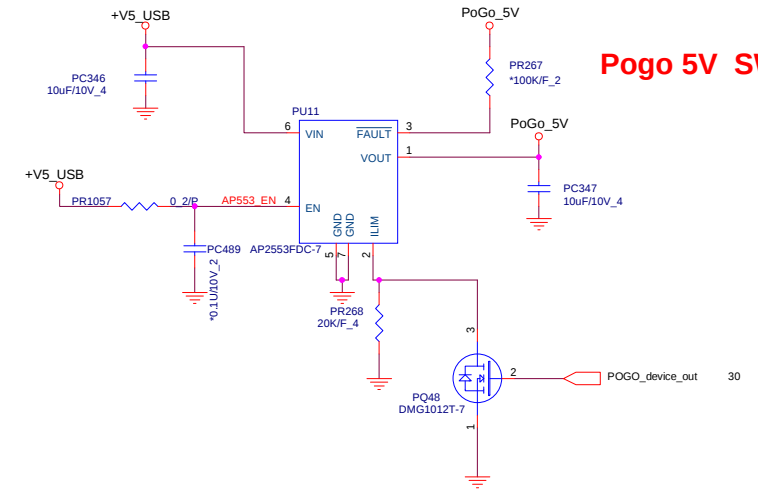
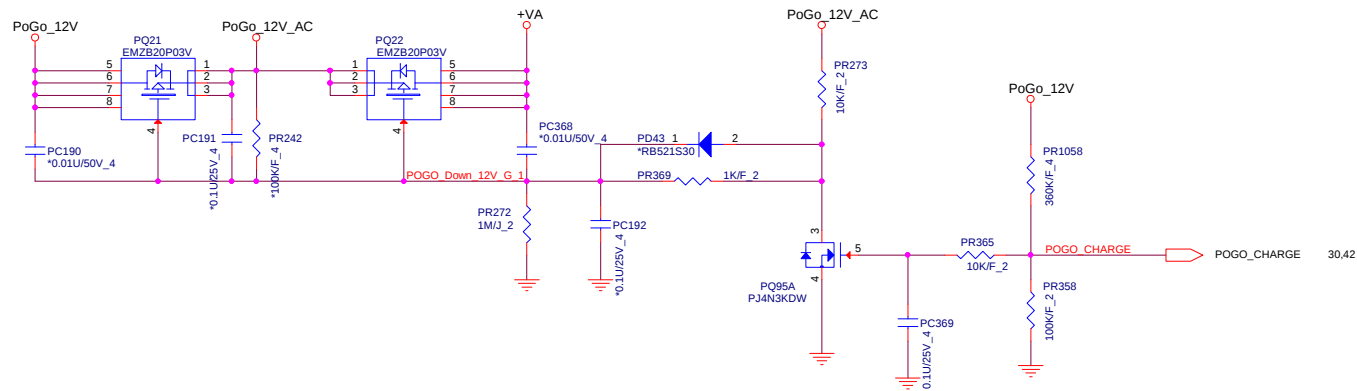
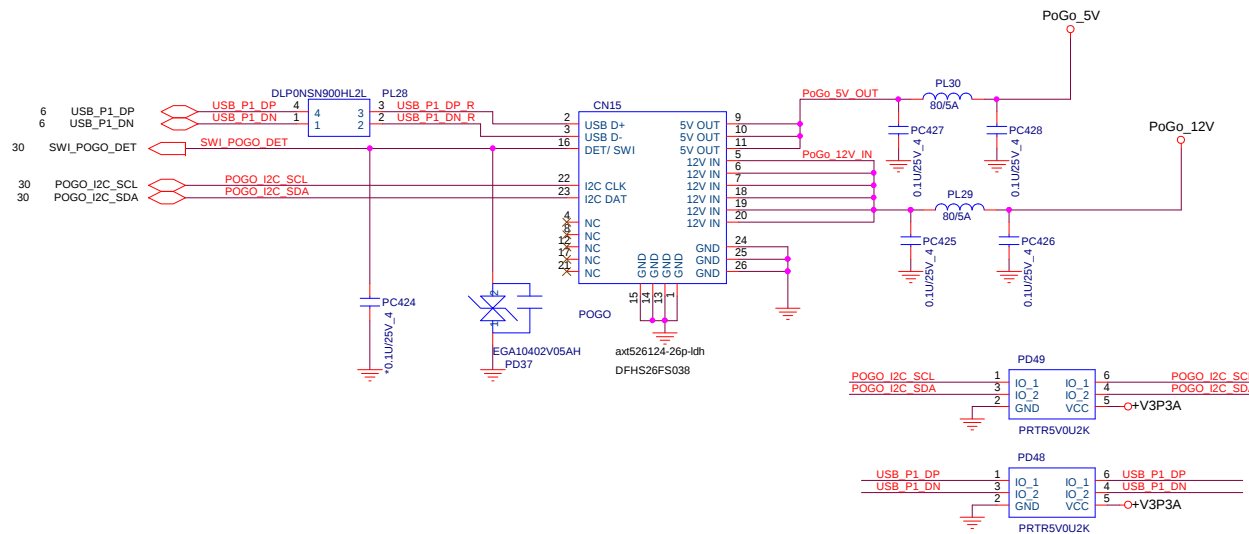
PROJECT : Eagle
Quanta Computer Inc.

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SWI_POGO_DET=1V~3V **SW5 on**

