

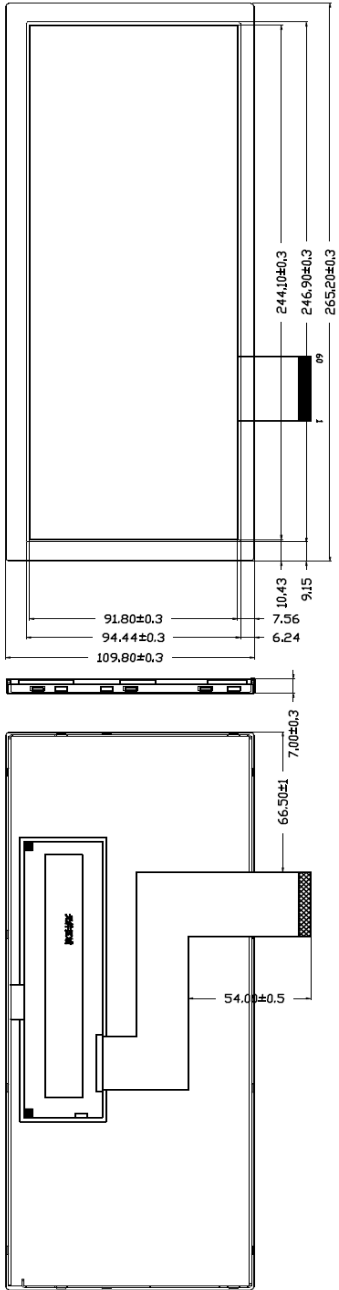
CUSTOMER	
MODEL NUMBER	JLAUO10250003
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
PREPARED BY			
CHECKED BY			
APPROVED BY			
QUALITY BY			

DISTRIBUTION LIST: MARKETING

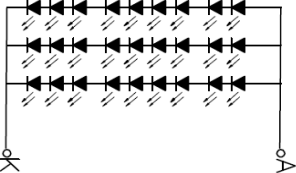
NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	1280 (H)×480(V)	
2	Active Area	mm	243.84(H)×91.4(V)	
3	Screen Size	inch	10.25(Diagonal)	
4	Dot Pitch	mm	0.0635(H)×RGBx0.190.5(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	Colors	
7	Overall Dimension	mm	261.65 x 110.37 x 8.73/16.23 w/o Boss, w BOSS	Note 2
8	Weight	g	450+/-10%	
9	Display Mode	--	Normally Black	
10	Surface Treatment		AG + 3H	

Customer Code.:			SPECIFICATION OF BACKLIGHT	
CUSTOMER'S P/N:			EDITION: 01	
Date: 2018.12.16	Page: 1/1	THE THIRD ANGLE	FX'S P/N(exclude wrapper):	FXS P/N:
			(include wrapper)	
			Approval(核准)	
			Check (检查)	
			Design(设计)	



- Notes:
- Unit:mm.
 - Do not scale drawing.
 - All radii without dimension R0.2.
 - ΔModification Mark.
 - draft angle: 1°
 - Backlight luminance : 450d/m²(typ)
 - Luminance uniformity: 80%(min)/(max*100%)
 - UnSpecified Tolerance is ±0.2
 - Operation conditions : If=210mA, Vf=23~31(MAX)

Backlight 27LED Circuit



- 10.All materials comply with RoHS
- 11.The measured value of luminance and color coordinate bases FX's BM-7
- 12.Check item:1~9

REV	DATE	DESCRIPTION (修改内容)	REVISERNO.	TITLE	Quantity
1					1
2					1
3					1
4					1
5					1
6					1
7					1
8					1
9					1
10					1
11					1
12					1

Customer:	Approval Date:	Confirm Date:	Approval by:	Confirm
1	2	3	6	7
弘瑞明光电有限公司 HONGRUI MING OPTOELECTRONIC CO., LTD.				

3. Interface Signals

Table 2: Pin Assignments for the LCD Connector

Pin No.	Symbol	Description	Remarks
1	AGND	Ground	
2	NC	No connect	
3	DVDD	Power pin	3.3V typ.
4	GND	Ground	
5	NC	No connect	
6	DVDD	Power pin	
7	GND	Ground	
8	NC	No connect	
9	NC	No connect	
10	NC	No connect	
11	NC	No connect	
12	NC	No connect	
13	NC	No connect	
14	NC	No connect	
15	GND	Ground	
16	DVDD	Power pin	
17	GND	Ground	
18	PIND3	Positive LVDS differential data input 3+	
19	NIND3	Negative LVDS differential data input 3-	
20	GND	Ground	
21	PINC	Positive LVDS differential clock input CLK+	
22	NINC	Negative LVDS differential clock input CLK-	
23	GND	Ground	
24	PIND2	Positive LVDS differential data input 2+	
25	NIND2	Negative LVDS differential data input 2-	
26	GND	Ground	
27	PIND1	Positive LVDS differential data input 1+	
28	NIND1	Negative LVDS differential data input 1-	
29	GND	Ground	
30	PIND0	Positive LVDS differential data input 0+	
31	NIND0	Negative LVDS differential	

Pin No.	Symbol	Description	Remarks
		data input 0-	
32	GND	Ground	
33	GND	Ground	
34	GRB	Global reset pin	
35	STBYB	Standby mode	L: Standby H: Normal
36	NC	No connect	
37	DVDD	Power pin	
38	NC	No connect	
39	GND	Ground	
40	NC	No connect	
41	NC	No connect	
42	NC	No connect	
43	GND	No connect	
44	DVDD	Power pin	
45	GND	Ground	
46	NC	No connect	
47	NC	No connect	
48	NC	No connect	
49	NC	No connect	
50	NC	No connect	
51	NC	No connect	
52	NC	No connect	
53	GND	Ground	
54	DVDD	Power pin	
55	SELB	6bit/8bit mode select	
56	VGH	Positive power for TFT	
57	DVDD	Power pin	
58	VGL	Negative power for TFT	
59	GND	Ground	
60	BIST	BIST	

•Optical specifications (Note 1, 2)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response	Tr+Tf	$\theta=0^\circ, 25^\circ\text{C}$	-		40	ms	Note 3
		$\theta=0^\circ, 0^\circ\text{C}$	-		80		
		$\theta=0^\circ, -20^\circ\text{C}$	-		200		
		$\theta=0^\circ, -30^\circ\text{C}$	-		400		
Contrast ratio	CR	$\theta=0^\circ$	800		-		Note 4, 5, 6
Viewing Angle Top Bottom Left Right		$CR \geq 10$	70 70 70 70	80 80 80 80	- - - -	deg.	Note 7, 8

•Reliability Test Items (Note 2)

No.	Test items	Conditions		Remark
1	High temperature storage	Ta=	240Hrs	Note1
2	Low temperature storage	Ta=	240Hrs	
3	High temperature operation	Ta=	240Hrs	
4	Low temperature operation	Ta= -	240Hrs	Note1, 3
5	High temperature and high humidity	Ta= , 90% RH	240Hrs	Operation
6	Heat shock	~/100 cycles 1Hrs/cycle		Non-operation
7	Electrostatic discharge	Contact = ± 8 kV, class B (R=330 Ω ,C=150pF) Air = ± 15 kV, class B (R=330 Ω ,C=150pF) 1 times for each point.		Operation (Note 4)

3.7 Electrical interface

3.7.1 Supply voltage and current

Requir. Ref.	Parameter	Symbol	Condit ions	MIN	TYP	MAX	Unit	Remarks
3.4.1.1	Power Supply Voltage	V_{CC}		3.0	3.3	3.6	V	
3.4.1.2	Power Supply Current	I_{CC}	White pattern	–	td	350	mA	Note 4-5-1
3.4.1.3	Power Consumption	P_{CC}		–	td	1.3	W	
3.4.1.4	Inrush Current	I_{RUSH}		–	–	1.5	A	For reference, Note 4-5-2
3.4.1.5	Input Signal Voltage	V_H	HVR, PDC, Bit_Sel	$0.7 V_{CC}$	–	V_{CC}	V	Note 4-5-3
3.4.1.6	Input Signal Voltage	V_L		0	–	$0.3 V_{CC}$	V	
3.4.1.7	Permissive input ripple	V_{RF}		–	–	200	mV _{PP}	

Table 3-10 Supply voltage and current

Note 4-5-1 The specified current and power consumption are measured at $V_{CC}=3.3V$, $T_A=25 \pm 2^\circ C$, $f_V=60Hz$, white pattern)

Note 4-5-2 For reference: The duration of rush current is about 2ms, rising time of power input is minimum 0.5ms ($V_{CC}=3.3V$, $T_A=25 \pm 2^\circ C$, $f_V=60Hz$)

Note 4-5-3 The recommended operating conditions show the ranges in which the device can operate normally. Operation beyond the limit of the recommended operation conditions is not assured, even though operating conditions are within the limit of the maximum ratings.

Note 4-5-1 The specified current and power consumption are measured at $V_{CC}=3.3V$, $T_A=25 \pm 2^\circ C$, $f_V=60Hz$ (pattern)

Note 4-5-2 For reference: The duration of rush current is about 2ms, rising time of power input is minimum ($V_{CC}=3.3V$, $T_A=25 \pm 2^\circ C$, $f_V=60Hz$)

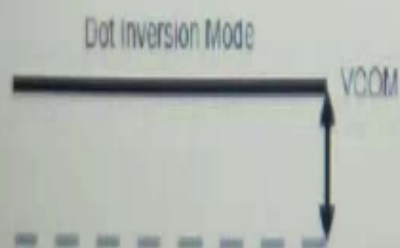
Note 4-5-3 The recommended operating conditions show the ranges in which the device can operate normally. Operation beyond the limit of the recommended operation conditions is not assured, even though the operating conditions are within the limit of the maximum ratings.

3.7.2 VCOM

Vcom adjustment has to be done at EOL at supplier.

3.7.2.1 VCOM adjustment step

We recommend keeping the VCOM adjustment step less than 20mV in case using a digital adjustment. High resolution voltage step is more adjustable to the optimum VCOM. It brings out the best optical performance of LCD.



Adjustment Step

Should be smaller than 20mV

3.7.2.2 VCOM adjustment conditions

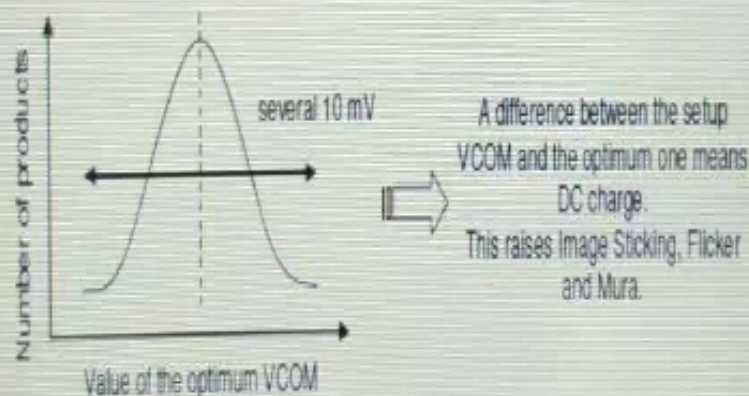
(For reference only)

- Ambient Brightness < 10 Lux
- Backlight PWM = 100%
- If the display includes V_{COM} circuitry and V_{COM} adjustment is performed during display production, then at least 9 positions according VESA standard need to be considered for adjustment procedure.

3.7.2.3 VCOM adjustment individually

The VCOM of all LCD modules should be adjusted individually.

Because there is the variation of the value of optimum VCOM at each LCD module.



The value of the VCOM means voltage level of COM signal. In dot inversion mode, it means DC voltage level of the COM signal.

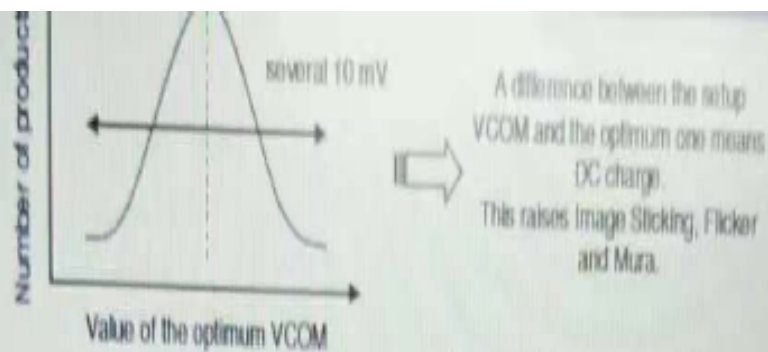
3.7.2.4 VCOM adjustment pattern and detection position

It is recommended to use following patterns for VCOM adjustment.

For dot inversion: 1 sub-pixel checker pattern with 0/63 and 32/63. (see the following figure)

For VCOM adjustment, detect at the center of the display by flickering measuring equipment.

The above method is the same condition as our QA standard



The value of the VCOM means voltage level of COM signal. In dot inversion mode, it means DC voltage level of the COM signal.

3.7.2.4 VCOM adjustment pattern and detection position

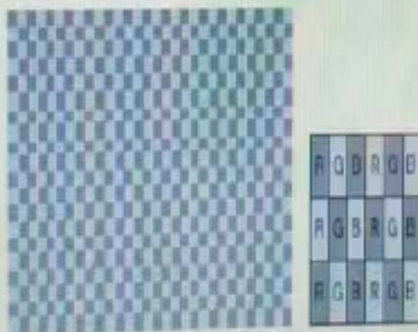
It is recommended to use following patterns for VCOM adjustment.

For dot inversion: 1 sub-pixel checker pattern with 0/63 and 32/63. (see the following figure)

For VCOM adjustment, detect at the center of the display by flickering measuring equipment.

The above method is the same condition as our QA standard.

All shipment LCD modules are adjusted by this standard.



Dot Inversion Driving
(1 Sub-pixel Checker Pattern)

3.7.2.5 VCOM temperature characteristic

VCOM drift over temperature has to be characterized during development.

Example for VCOM drift evaluation result (tbd. mV / K) to be provide by the supplier.

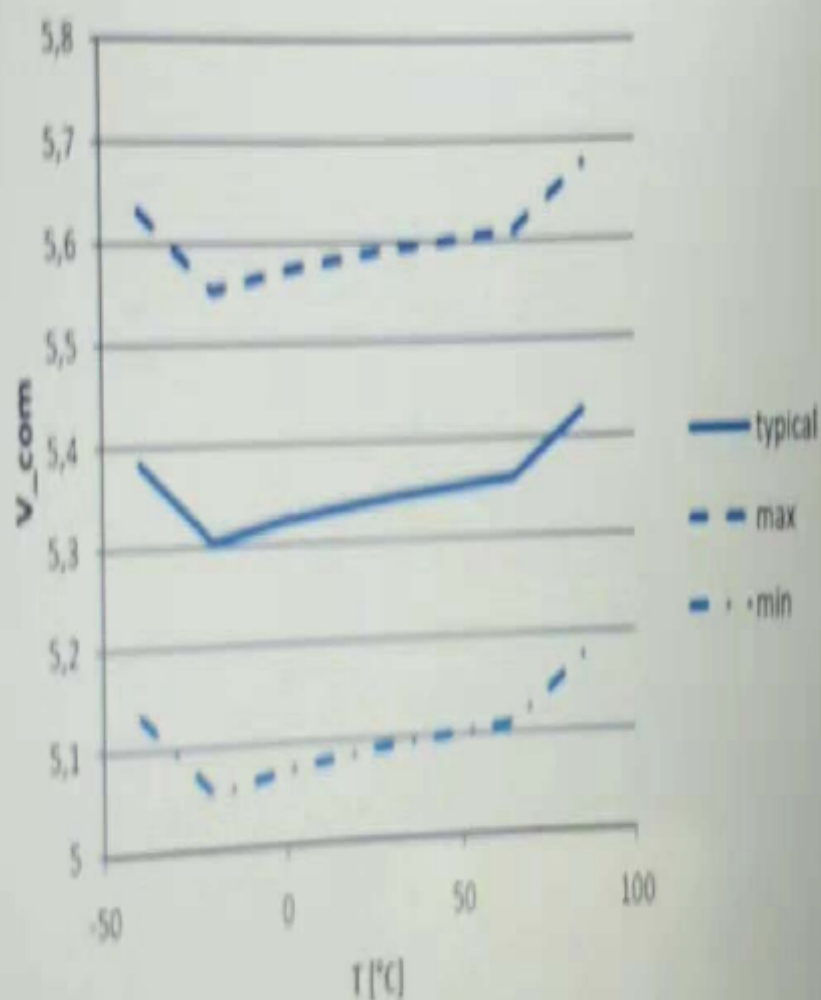


Figure 3-1: VCOM drift evaluation result (example, supplier has to provide actual data)

3.7.3 Gamma

3.7.3.1 Adjustment

Gamma adjustment has to be done at EOL at supplier. Supplier must provide a detailed adjustment procedure with resolution and bandwidth.

3.7.3.2 Gamma Curve

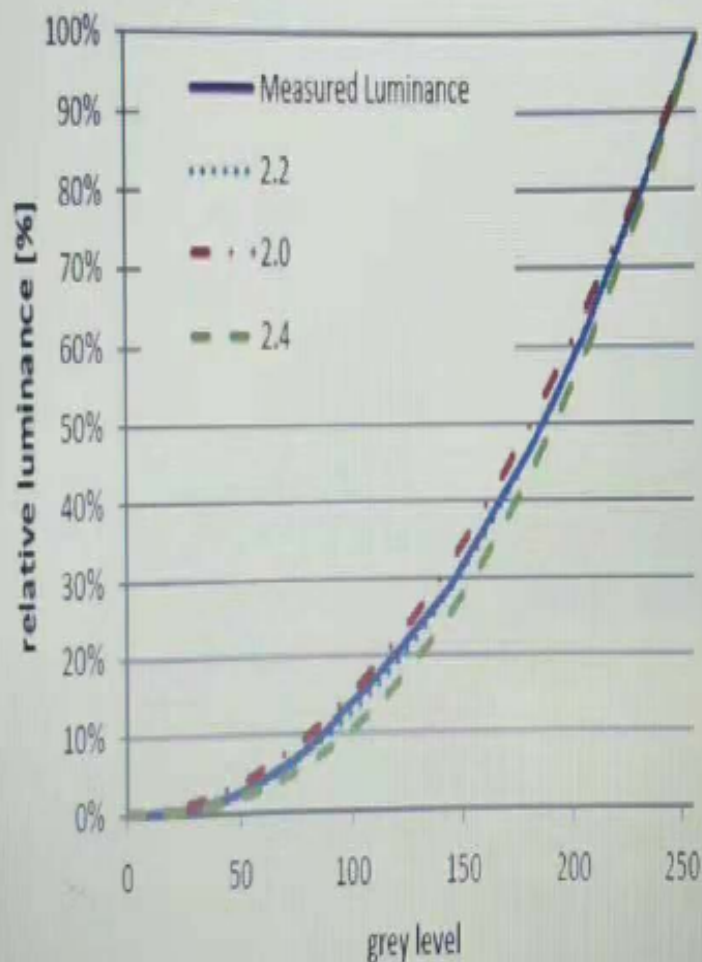


Figure 3-4 Relative luminance of 256 grey levels versus theoretical gamma curves (2.0, 2.2, and 2.4)
(example, supplier has to provide actual data)

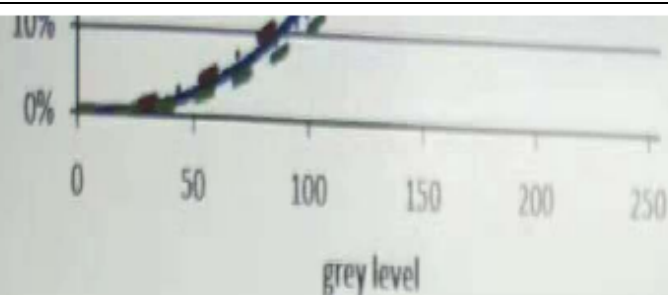


Figure 3-4 Relative luminance of 256 grey levels versus theoretical gamma curves (2.0, 2.2, and 2.4)
(example, supplier has to provide actual data)

3.8 Power on/off sequence

Requir. Ref.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
3.5.1	Power On	t_1		tbd		ms	see figure 6
3.5.2	Power On	t_2		tbd		ms	see figure 6
3.5.3	Power On	t_3		tbd		ms	see figure 6
3.5.4	Power On	t_4		tbd		ms	see figure 6
3.5.5	Power Off	t_5		tbd		ms	see figure 6
3.5.6	Power Off	t_6		tbd		ms	see figure 6
3.5.7	Power Off	t_7		tbd		ms	see figure 6
3.5.8	Power Off	t_8		tbd		ms	see figure 6

Table 3-1 Timing requirements power up and down sequence

The supplier has to define the power up and down sequence in the VA.

3.9 Timing Panel Interface

3.9.1 Interface Timing (1280 x 480 / 75 Hz)

Requir. Ref.	Item	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
3.6.1.1	DotClk	Frequency	$1/T_C$	Tbd	60.48	tbd	MHz	
3.6.1.2	Horizontal	Period Area	T_H	Tbd	1536	tbd	DotClk	
3.6.1.3	Horizontal	Blanking Area	T_{HB}	Tbd	256	tbd	DotClk	
3.6.1.4	Horizontal	Display Area	T_{HD}	1280	1280	1280	DotClk	
3.6.1.5	Vertical	Period Area	T_V	Tbd	525	tbd	lines	
3.6.1.6	Vertical	Blanking Area	T_{VB}	Tbd	45	tbd	lines	
3.6.1.7	Vertical	Display Area	T_{VD}	480	480	480	lines	
3.6.1.8	Framerate			75	75	75	Hz	

Table 3-12 Timing

3.9.2 LVDS Interface DC Characteristic

Requir. Ref.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
3.6.2.1	Differential input high threshold	V_{THLV}	-	-	50	mV	$V_{CMLV} = 1.2V$
3.6.2.2	Differential input low threshold	V_{TLV}	-50	-	-	mV	$V_{CMLV} = 1.2V$
3.6.2.3	LVDS common mode voltage	V_{CMLV}	1.0	1.2	1.5	V	
3.6.2.4	LVDS input voltage	V_{INLV}	0.7	-	1.8	V	
3.6.2.5	LVDS input voltage				$1V <$		

3.6.1.7	Vertical	Display Area	T_{VD}	480	480	480	lines	
3.6.1.8	Framerate			75	75	75	Hz	

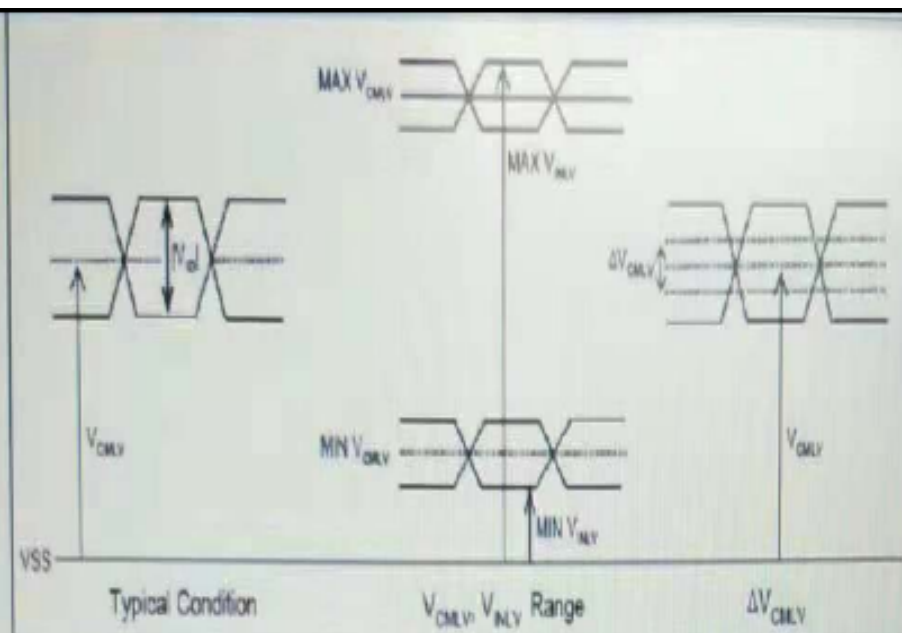
Table 3-12 Timing

3.9.2 LVDS Interface DC Characteristic

Requir. Ref.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
3.6.2.1	Differential input high threshold	V_{THLV}	-	-	50	mV	$V_{CMLV} = 1.2V$
3.6.2.2	Differential input low threshold	V_{TLLV}	-50	-	-	mV	$V_{CMLV} = 1.2V$
3.6.2.3	LVDS common mode voltage	V_{CMLV}	1.0	1.2	1.5	V	
3.6.2.4	LVDS input voltage	V_{INLV}	0.7	-	1.8	V	
3.6.2.5	Δ LVDS common mode voltage	ΔV_{CMLV}	No limit	mV	$1V < V_{CMLV} < 1.5V$		
3.6.2.6	Δ LVDS common mode voltage	ΔV_{CMLV}	-	-	250	mV	$V_{CMLV} \leq 1V$ or $V_{CMLV} \geq 1.5V$
3.6.2.7	Differential input voltage	$ V_{ID} $	350	450	600	mV	
3.6.2.8	Input current	I_{INLV}	-	-	± 20	μA	
3.6.2.9	LVDS internal termination resistor	R_{TERMLV}	80	100	120	Ω	

($V_{DD_IF}=V_{DD}=3.0V$ to $3.6V$, $V_{DDA} = 8V$ to $13.5V$, $GND_IF=GND=GND_A=0V$, $T_A=-40^{\circ}C$ to $85^{\circ}C$)

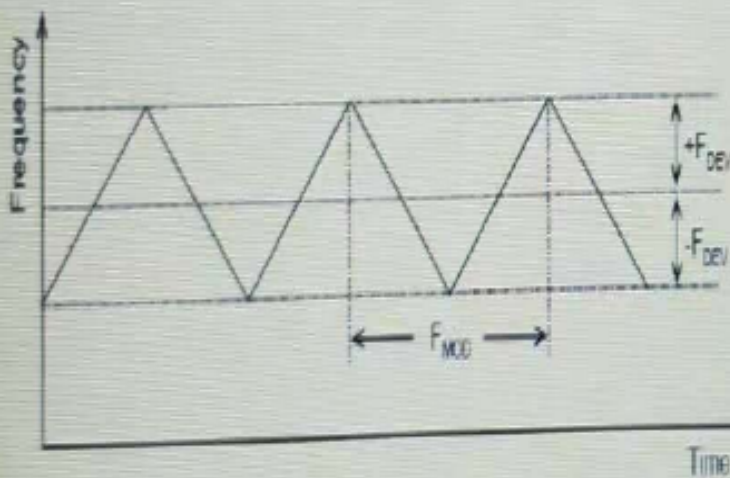
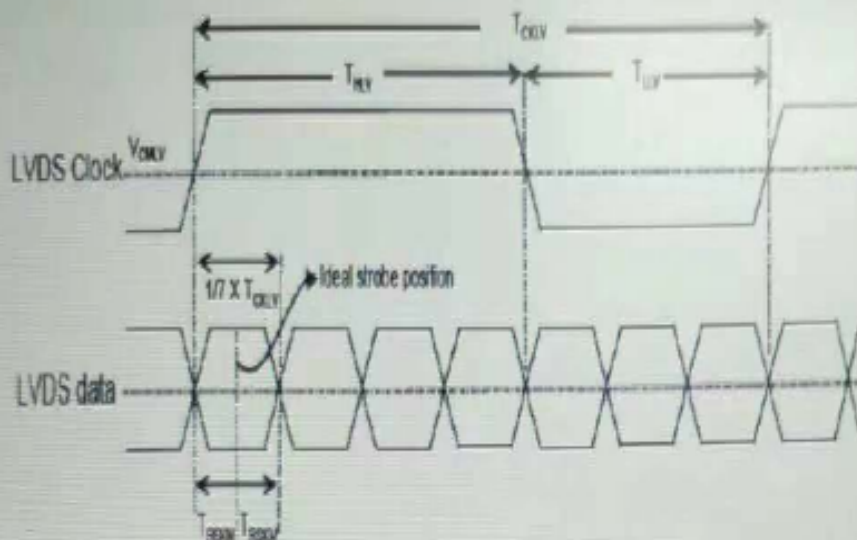
Table 3-13: Interface DC Characteristic



3.9.3 LVDS Interface AC Characteristic

Requir. Ref.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
3.6.3.1.1	Input data position for Bit0	TRIP0	-	0	-	ns	
3.6.3.1.2	Input data position for Bit1	TRIP1	-	1/7 T	-	ns	
3.6.3.1.3	Input data position for Bit2	TRIP2	-	2/7 T	-	ns	
3.6.3.1.4	Input data position for Bit3	TRIP3	-	3/7 T	-	ns	
3.6.3.1.5	Input data position for Bit4	TRIP4	-	4/7 T	-	ns	
3.6.3.1.6	Input data position for Bit5	TRIP5	-	5/7 T	-	ns	
3.6.3.1.7	Input data position for Bit6	TRIP6	-	6/7 T	-	ns	
3.6.3.1.8	LVDS output clock period	RCOP	-	T	-	ns	
3.6.3.1.9	LVDS output clock high time	RCOH	0.45 T	0.5 T	0.55 T	ns	
3.6.3.1.10	LVDS output clock low time	RCOL	0.45 T	0.5 T	0.55 T	ns	

Table 3-14: Interface AC Characteristic



3.9.4 LVDS data input format (8 bit)

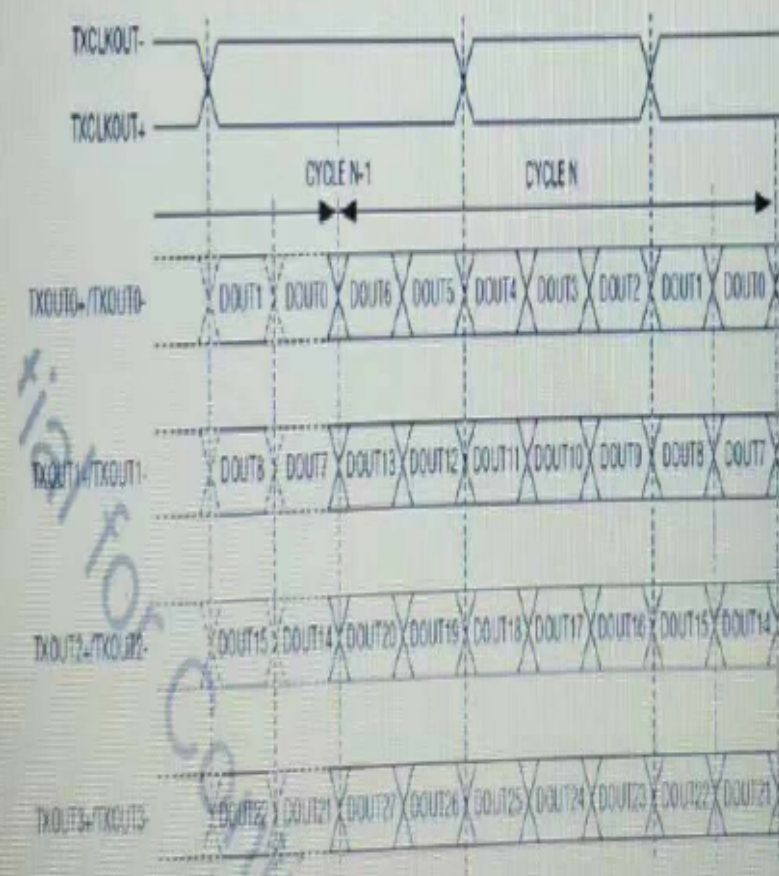
The interface is formed by five differential signal pairs:
 4 pairs for data transmission
 1 pair for clock transmission

3.9.4 LVDS data input format (8 bit)

The interface is formed by five differential signal pairs:

4 pairs for data transmission

1 pair for clock transmission



3.9.6 Timing Panel Interface

The display must be able to be operated with a frame frequency of 75Hz.

3.9.7 Timing and modulation requirements

For EMI optimization, a modulation of the pixel clock frequency (and all data and synchronization signals controlled by pixel clock frequency) is required. At least $\pm 5\%$ jitter for all signals are possible over the complete operation range (see figure 3-3)

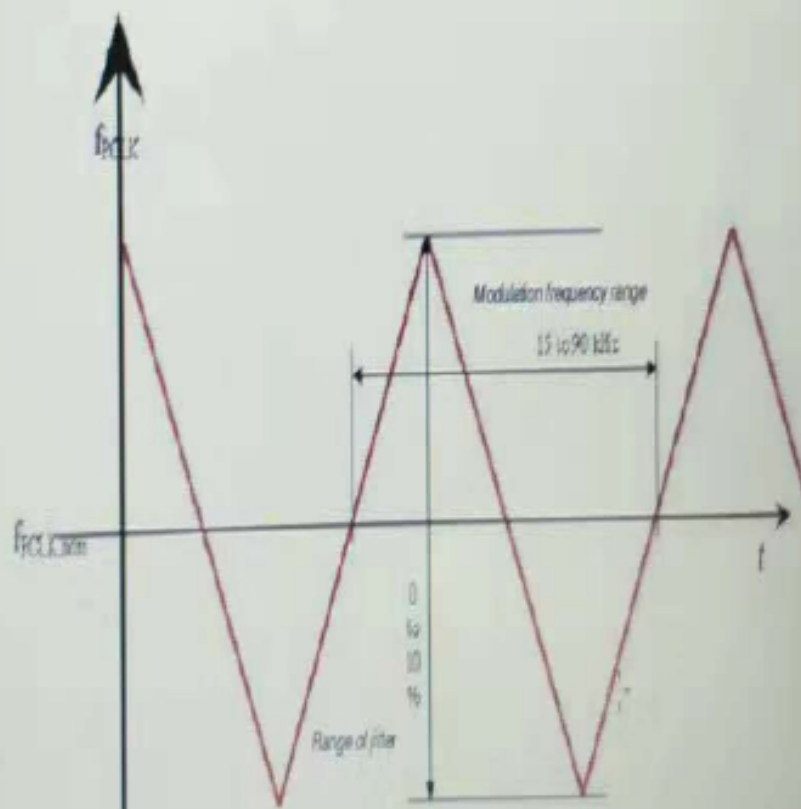
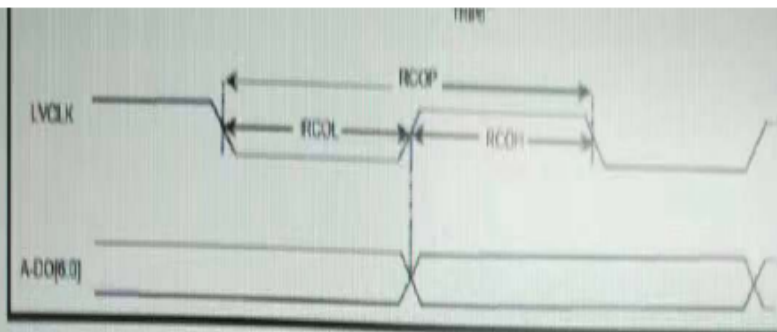


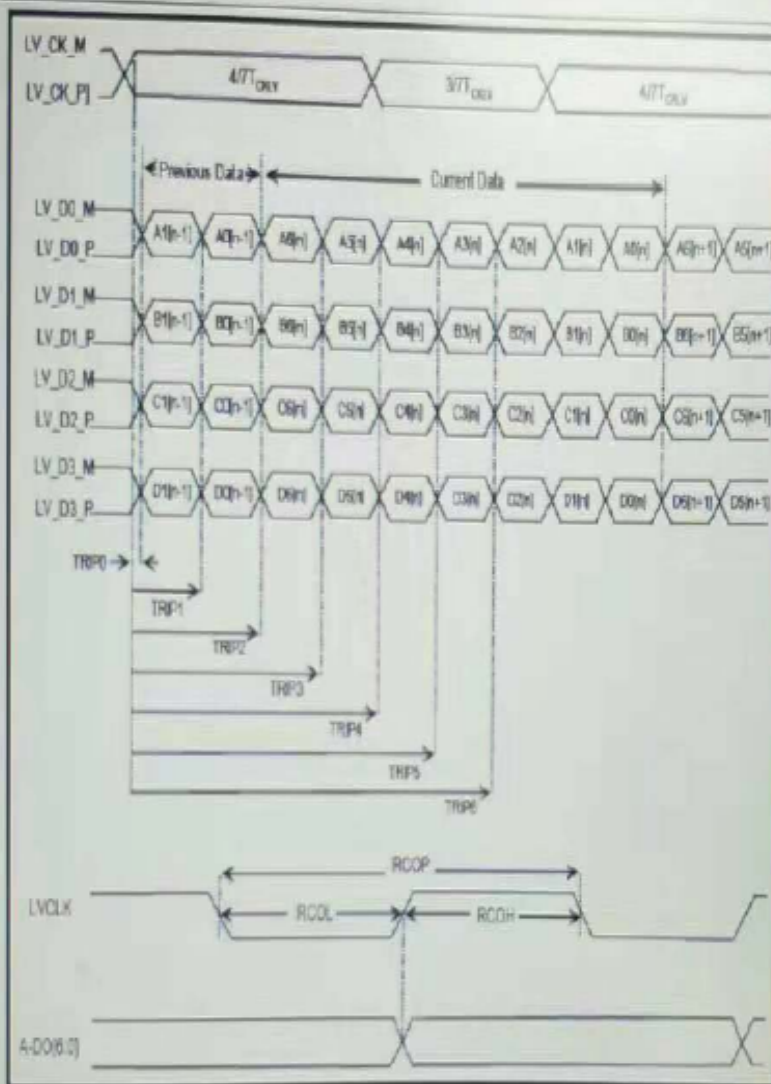
Figure 3-3 Example of SSCG modulation of clock frequency for reference

The display has to show full functionality for the defined modulation frequency range and range of jitter. Data setup and data hold time of signal is according table 3-14 (AC specification for source driver IC).



Requir. Ref.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
3.6.3.2.1	Input clock period	T_{CKLV}	19.2	-	35.2	ns	
3.6.3.2.2	Input clock high period	T_{HLV}	3/7	-	4/7	T_{CKLV}	
3.6.3.2.3	Input clock low period	T_{LLV}	3/7	-	4/7	T_{CKLV}	
3.6.3.2.4	Receiver skew margin	T_{RSKM}	-600	-	600	ps	$20 \text{ MHz} \leq F_{CKLV} \leq 60 \text{ MHz}$
3.6.3.2.5	Receiver skew margin	T_{RSKM}	-400	-	400	ps	$60 \text{ MHz} < F_{CKLV} \leq 85 \text{ MHz}$
3.6.3.2.6	Maximum input SSC modulation ratio	F_{DEV}	-3	-	3	%	
3.6.3.2.7	Maximum input SSC modulation frequency	F_{MOD}	-	-	200	kHz	

Table 3-15: Interface clock characteristics



Requir. Ref.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
3.6.3.2.1	Input clock period	T_{CKLV}	19.2	-	35.2	ns	
3.6.3.2.2	Input clock high period	T_{HLV}	3/7	-	4/7	T_{CKLV}	
3.6.3.2.3	Input clock low period	T_{LLV}	3/7	-	4/7	T_{CKLV}	

20 MHz < f_{CLK}

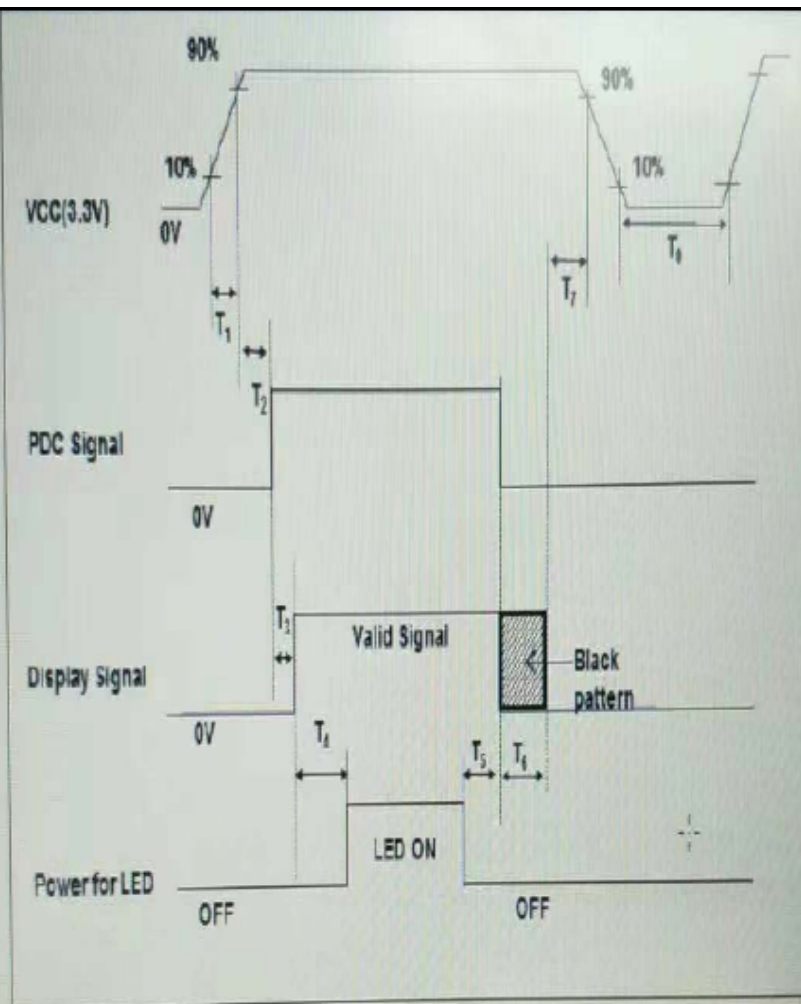


Figure 2: power up and down sequence

Black pattern will be send by Continental SW